TV750
PC/104 High Performance
VGA Graphics Board

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Contents

INTRODUCTION

1.1 OVERVIEW

This manual provides detailed technical information on the TV750 VGA graphics controller board designed for the PC/104 bus. The TV750 contains a high performance VGA controller sub-system, capable of driving a CRT and flat panel display simultaneously. The TV750 supports noninterlaced CRT displays with a resolution of up to 1024 x 768 with 256 colours. The TV750 directly drives monochrome LCDS, colour LCDs (both TFT and STN styles), electroluminescent (EL) and plasma displays. The TV750 comes with 512k byte of DRAM installed as standard. The TV750-1M version comes with 1M byte of DRAM installed.

A single 50 way rignt angled pin header provides access to the signals required for all displays.

1.2 TV750 FEATURES

- **65535 high performance VGA controller chip**
- **Drives CRT and flat panel displays simultaneously**
- **512K & 1Mbyte versions available**
- **Programmable frequency synthesiser**
- **16 and 24 bits per pixel colour options**
- **On board Vee generator for monochrome LCDs**
- **On board BIOS EPROM**
- **Single +5V power supply**
- **PC/104 V2.2 bus compatible**

TV750 VGA GRAPHICS CONTROLLER

2.1 65535 VGA CONTROLLER CHIP

Chips and Technologies use the name “Vampire” to describe a family of devices including the 65535 graphics chip which is fitted on the TV750.

The use of the 65535 chip allows the TV750 to drive the vast majority of currently available displays. The TV750 can drive CRTs or flat panels of many types, or a CRT and flat panel simultaneously.

The 65535 chip is a modern high performance VGA controller chip. As well as the standard VGA registers it has a large number of proprietary registers defined by Chips and Technologies which allow access to its extended features.

Chips and Technologies provide a comprehensive set of tools to generate new versions of the BIOS and debug the 65535 sub-system. These are provided free of charge in the form of evaluation software. In addition DSP Design have entered into licence agreement with Chips to allow us access to the full release versions of the software. The only practical difference between the evaluation software and the full release software is the BIOS generated by the evaluation software carries a message identifying it as evaluation software.

The BIOS editing tools will allow software engineers to customise the BIOS as required. See section 3 for more details about the VGA software available.

2.2 FREQUENCY SYNTHESISER

The 65535 features an internal frequency synthesiser. The synthesiser can be programmed by software to produce a wide range of dot clock rates as well as a range of frequencies to drive the memory timing. The clock frequencies are set by the VGA BIOS, and can be set with the BIOS editing program.

2.3 VIDEO MEMORY

The TV750 operates with 512K byte of video memory and the TV750-1M with 1 Mbyte to allow virtually all VGA formats to be supported.

The following table shows some extended video modes that are supported on the TV750 and the amount of video memory that is required for them to function. The standard VGA graphic modes 0H to 7H and 0DH to 13H require only 256k bytes of video memory.

Mode	Resolution	Colours	Video Memory
20H	640 x 480	16	512K
22H	800 x 600	16	512K
30H	640 x 480	256	512K
32H	800 x 600	256	512K
34H	1024 x 768	256	1M
40H	640 x 480	32,000	1M
41H	640 x 480	64,000	1M

Table 1: Typical TV750 Resolutions

2.4 ANALOGUE CRT INTERFACE

The CRT interface provides analog R, G and B signals as well as TTL level HSYNC and VSYNC signals. The CRT interface is the same as appears in desk-top PCs. Standard 15 pin VGA monitors can be connected to the TV750 either by using the TV750-CRTCAB cable manufactured by DSP Design or by making your own cable using table 2 below as a guide.

The analog R, G and B lines are terminated on the TV750 with 150 ohm resistors to GND. The CRT signals are present on connector J3.

J3		15 Pin VGA Connector
Pin No	Signal Name	
1	Gnd	6
2	Red	1
3	Gnd	7
4	Green	2
5	Gnd	8
6	Blue	3
7	Gnd	10
8	Hsync	13
9	Gnd	5 *
10	Vsync	14

Table 2: Connections for a VGA CRT

* NOTE: Pin 5 of the 15 pin VGA connector is the self test pin. This should be connected to ground as indicated above.

2.5 FLAT PANEL INTERFACE

The 65535 chip can drive one of many types of flat panel. If desired the flat panel can be driven simultaneously with a CRT. The flat panel signals are available on connector J3.

The 65535 chip can be programmed to operate with a wide range of flat panels. Two things need to be done to connect a given flat panel - the panel needs to be wired to the TV750 correctly and the BIOS needs to be modified to produce the required timing on the 65535 pins.

The function of the flat panel signals from the 65535 chip change as different panels are selected. Almost all panels can be driven directly by the signals available on the J3 connector.

The 65535 chip data sheet identifies the functions of the signals for different flat panels, and shows possible timing diagrams for a large range of flat panels, as well as wiring information for these panels.

The TV750 Utilities disk contains a number of pre-configured BIOSes and pre-configured BMS files for use with a wide range of flat panel displays. See the TV750 Utility disk for more up-to date information.
The VGA BIOS editing program, BMP535.EXE, can be run to configure the BIOS for the other flat panels. In many cases this will simply be a matter of running the BMP535 program and reading in one of a number of files with a .BMS file name. These files are each pre-configured for one type of flat panel, and have the effect of changing registers within the 65535 chip to values required by the display.

It is the intention of DSP Design to update the TV750 Utilities disk with additional BMS files periodically. See the TV750 Utilities disk for more up-to date information.

If no pre-configured BIOS or BMS file exists for the flat panel display you are using you will be required to obtain the data sheet for your display so that you can edit the BIOS to suit the display. See section 3 for more details on using the BIOS editing software.

2.6 Vee GENERATION

Vee is the negative voltage used to drive monochrome LCD displays.The Vee output can be set with the on-board potentiometers VR1 and VR2. VR1 sets the Vee voltage level. By adjusting VR1 a negative voltage (Vee) of between about -10V and -23V can be set. This is normally only adjusted once, and is set to the value specified in the LCD data sheet.The second potentiometer VR2 connects between GND (0V) and Vee, and is used to adjust the contrast level on most LCDs (Vo). Note that some LCDs do not have a Vo pin. The Vee generator can source currents in excess of 40mA. This should be adequate for almost all LCDS.

The Vee generator is based around a Maxim MAX749 LCD bias voltage supply chip. This chip has two pins which can be used to turn on and off the Vee supply. They can also be used to adjust the Vee voltage under software control, with some external hardware.

Most users will not want to adjust Vee by software. For this purpose the MAX749 control pins have been connected so that the Vee supply is turned on and off by the ENAVEE power sequencing pin. See section 2.7 for more information on power sequencing.

Users who want to disable the on-board Vee supply should connect the ADJVEE pin on J3 (pin 15) to GND. This will not be necessary for the CRT-only BIOS (134043.BO2), as Vee is disabled by default.

It is possible to adjust the Vee generator under software control, by driving the ENABLEVEE and ADJVEE pins from external I/O pins, which in turn could be controlled by software. Note that users will need to provide two suitable signals to drive the ENABLEVEE and ADJVEE pins and will need to write their own code to drive them.

The ADJVEE pin allows adjustment of the Vee output voltage when ENABLEVEE is high. The output voltage is controlled from 33% to 100% of the full scale output by a 64 step DAC counter internal to the Vee generator. On power-up or after a counter reset, the counter sets the DAC output to mid-range, that is 66.5% of full scale output. Each rising edge of ADJVEE increments the DAC counter. When incremented beyond full scale the counter rolls over and sets the DAC counter to the minimum value. In this way a single pulse applied to ADJVEE increases the DAC set point by one step, and 63 pulses decreases the set point by one step.

Example:

The DAC counter is set to mid-value (after power-up or a counter reset - see table below). VR1 is adjusted so that Vee measures -20V. Since the DAC counter has been set at mid value, Vee is only at 66.5% of the maximum Vee output attainable, so the full scale output that can be produced is approximately -30.1 V and the minimum is approximately 9.9V. Therefore a single DAC step would produce a change in Vee of:

((Full scale / 100) Adjustable Percentage Of Full Scale) / Number Of Steps

((30.1 / I 00) * 67 / 64 = 0.32V Per Step (Approx)

The ADJVEE and ENABLEVEE inputs control the DAC counter as shown in the table below. When

both these pins are low the Vee generator is shut down. When ENABLEVEE is low and ADJVEE is high the DAC counter is reset to mid-scale and the Vee generator turns on. When ADJVEE is low the counter does not change so long as power is kept applied to the TV750. The ADJVEE pin is pulled high by the ENAVEE pin on the 65535 chip as part of its power sequencing process. ENABLEVEE is pulled low via a 10k ohm resistor on the TV750.

ADJVEE	ENABLEVEE	Result
Low	Low	Vee generator shut down
High	Low	Reset DAC counter to mid range
X	High	On
↑	High	Increment counter by one

For a full operational description of the MAX749 you will need to obtain a copy of the MAX749 data sheet from Maxim.

2.7 POWER SEQUENCING

Two outputs from the 65535 chip are available on the J3 connector, to sequence power supplies on a flat panel. The ENAVEE signal is intended to enable an external Vee generator for LCDS. The ENAVDD signal is intended to switch on and off the +5V supply to flat panels. This can be useful if power conservation is important and many displays demand that the Vee power supply is properly sequenced to prevent damage.

During power-down the ENAVEE signal is taken inactive.The flat panel timing and data signals are then taken to their inactive state shortly afterwards, at a time defined by register XR5B, and then the ENAVDD signal is taken inactive, again after an interval defined by XR5B. During power up the sequence is reversed.

2.8 BACKLIGHT CONTROL

The TV750 provides two signals to enable power sequencing of the LCD backlight. These are the ENABKL and /BACKLIGHT pins on the J3 connector. The ENABKL pin is active high and has an 8mA drive limit. The /BACKLIGHT signal is active low and is a buffered version of ENABKL and is capable of sinking up to 100mA. It is recommended that the /BACKLIGHT pin be used in all cases.

The /BACKLIGHT signal on the J3 connector is available to allow power sequencing of the flat panel backlight voltage. This signal is in addition to the ENAVDD and ENAVEE signals described in section 2.7 above. During power-down the /BACKLIGHT signal goes high after ENAVEE goes inactive and before ENAVDD goes inactive. During power up this sequence is reversed.

The /BACKLIGHT signal can be used as part of a backlight controller circuit to switch a backlight on or off. Normally the /BACKLIGHT signal would drive an external transistor or relay, which in turn would switch on or off the backlight.

2.9 PC/104 BUS

The TV750 is PC/104 compliant. That is the TV750 conforms to both the electrical and mechanical specifications laid down by the PC/1 04 V2.2 document.

The TV750 makes use of the 16-bit data signals present on the J2 connector. Due to bugs in the 65535 silicon the TV750 may not operate correctly when used with an 8-bit processor. Contact DSP design if you wish to use a processor with an 8-bit bus (ie. only implementing the J1 signals).

The TV750 has been built around the PC/104 V2.2 specification. This includes the use of polarising

pins on the J1 & J2 connectors. Some earlier versions of the PC/104 specification did not use polarising pins and it was seen that this could result in possible mis-alignment and subsequent product failure if power was applied before the error was discovered. 'KEY'positions have been assigned to the J1 and J2 connectors. These can be seen on the J1 and J2 pin assignment tables in Appendix C.The'KEY'positions have had their pin removed and thesocket hole has been blocked to prevent entry by any adjacent pin.

Users should note that any boards produced to an earlier PC/104 specification will not mate with V2.2 boards. However it is quite simple to modify the J1 and J2 connectors to circumvent this problem.

3.1 BIOS FOR THE TV750

In PC compatible computers with VGA graphics two BIOSes are required: the main system BIOS and the VGA BIOS. The VGA BIOS is usually 32k bytes in length and is usually located at starting address C000:0.

The TV750 has a VGA BIOS socket (IC3) and is supplied as standard with a simultaneous CRT and flat panel display BIOS EPROM (134041.BO2) installed in the IC3 socket. Other BIOSes are available on the TV750 Utilities Disk.

Before installing the TV750 onto a PC/104 stack you must first consider the location of the VGA BIOS. If the VGA BIOS EPROM is to remain installed on the TV750 then the processor system BIOS must arrange for a 32k block of memory to be mapped onto the bus at address C000:0 The TC486 standard BIOS(185010.BOI) has C000:0 to C7FF:F mapped onto the bus for this very purpose.

Alternatively the processor system BIOS and the VGA BIOS can be combined and placed into a single EPROM, installed on the processor card, where the VGA BIOS would be addressed at segment C000:0. The TC486 BIOS EPROM (185011.BO1) has C000:0 to C7FF:F mapped onboard for this purpose.

3.2 SELECTING A SUITABLE VGA BIOS

The TV750 is shipped with a simultaneous CRT and flat panel BIOS EPROM as standard. This allows both a VGA CRT and a 640 x 480 mono LCD to display simultaneous images. This and a number of other preconfigured BIOSes as well a number of.BMS BIOS configuration files are available on the TV750 Utility disk.

For users not requiring flat panel support there is a CRT-only BIOS (134043.BO2). A suitable cable is available to connect the TV750 direct to a 15pin VGA CRT monitor. See Appendix F for Options and Ordering information. There is also an LCD-only BIOS (134042.BO2).

If the TV760 Utility disk does not contain a suitable BIOS or BMS file for your flat panel display type you will need to edit an existing BIOS. For information on editing existing BIOSes and loading preconfigured . BMS files see section 3.5 (VGA BIOS Editing Tools) and the TV750 Utility Disk.

3.3 INSTALLING THE VGA BIOS IN IC3

The VGA BIOS can be installed on the TV750 in the IC3 site. This is a 28 pin IC socket and accepts suitable 27C512 (64K byte) EPROM devices. The VGA BIOSes on the TV750 Utility disk are 32K bytes in length and should be programmed into the EPROM starting at offset zero. The BIOS image will fill the first 32k of the EPROM device.

When installing the video BIOS on the TV750 the following steps should be followed:

1 . Choose the TV750 BIOS that most suits your needs. This may be a pre-configured BIOS from the TV750 Utility disk or one that you have configured for yourself using the BMP535 editor.

2. Program the BIOS into the first half of the EPROM at offset zero.

3. Install the EPROM into the IC3 site on the TV750

4. Check that jumper area E1 is linked (2-3).

The processor system BIOS must map a 32K byte block of memory onto the bus starting at address C000:0. This will enable the TV750 BIOS can be accessed across the PC/104 bus. Any other graphics cards in the PC/104 system must be disabled.

3.4 COMBINING A SYSTEM BIOS AND VGA BIOS INTO ONE EPROM

DSP Designs processor boards allow the system BIOS and VGA BIOS to be combined in one EPROM. To combine the TV750 VGA BIOS and the processor system BIOS together in one EPROM, the following steps should be followed:

1 Choose a TV750 VGA BIOS that most suits your needs. This may be a pre-configured BIOS from the TV750 UTILS disk or one that you have configured for yourself using the BMP535 editor.

2. The system BIOS and EPROM that you choose must satisfy the following criteria:-

   The EPROM must have an unprogrammed 32k byte block available for the TV750 VGA BIOS code to reside.

   The system BIOS must map that 32k block onboard at address C000:0.

3. Using what EPROM programming technology you have at your disposal arrange the system BIOS and the VGA BIOS into the contents of the EPROM so that the system BIOS will be mapped onto address F000:0 and the VGA BIOS will be mapped at address C000:0.

4. If using ROM disks follow the instructions for installing the ROM disk driver and ROM disk code from the processor Technical Reference Manual.

5. Program the EPROM.

The resulting EPROM will contain both the system BIOS and the VGA BIOS and is ready to be installed into the BIOS EPROM socket on the processor card. The BIOS EPROM socket link or jumper settings must be set correctly for the size of EPROM used. If you have fitted a combined system and VGA BIOS on your processor card then you must remove the EPROM from the TV750 and set jumper E1 in the (1 -2) position.

3.5 VGA BIOS EDITING TOOLS

The VGA BIOS itself may be edited with the program from Chips and Technologies called BMP535.EXE. This program can be found on the TV750 Utility Disk. The BMP535 program acts on a file containing a copy of the VGA BIOS, It allows all of the registers within the 65535 chip to be modified, clock rates to be set and so on. Various files (with a BMS file name) contain pre-configured parameters to suite a range of flatpanel displays. These.BMS files can be read into the VGA BIOS file by the

BMP535 program and serve to modify a range of registers to suit particular displays. The TV750 Utility disk contains information describing the BMP535 tools and options.

Other registers in the 65535 chip can be changed by the BMP535 program to invoke special display modes. These include registers XR57 and XR58, which control vertical compensation, XR61 to XR63 which control text and graphics enhancement, and video polarity, and XR50 which control grey scale simulation. In addition the VGA BIOS can be configured for flat panel, CRT or simultaneous operation.

Note that to save users having to program an EPROM every time a modification is made to the VGA BIOS, a program called RAM535.EXE is provided. This is a version of the VGA BIOS which can be edited by the BMP535 editing program and then run from the DOS prompt. The RAM535 BIOS replaces the VGA BIOS from the EPROM, and the changes can be quickly evaluated.

The BMP535 program can save a complete set of register settings from a particular BIOS configuration. These register settings are saved as a BMS file. A BMS file can be read into a BIOS image by the BMP535 program as well. This allows, for instance, a development sequence such as this:

Run BMP535 with a pre-contgured VGA BIOS then save the register settings as a BMS file. Quit from BMP535 and re-run it, loading RAM535.EXE. Read in the BMS file previously saved, then make further changes to the BIOS. Save the modified RAMS35.EXE and test it on your processor board by typing “RAM535” at the keyboard. Make further changes as necessary to the RAM535.EXE version of the VGA BIOS. When the RAM535.EXE is correct, load it with BMP535, save the register settings as a BMS file, then re-run BMP535 with a EPROM version of the VGA BIOS and load into it the BMS file containing the register settings which had been successfully tried with the RAM535.EXE version. Save the resulting EPROM image and program it into an EPROM.

DSP Design have licenced the BMP535 software from Chips and Technologies, but are unfortunately not allowed to distribute the release version of this program to our customers. Chips do however allow us to distribute an evaluation copy on the TV750 Utilities Disks. The only difference is that various EVALUATION messages are displayed. The evaluation software can be used for development work, and customers are invited to contact DSP Design who will be able to use the release software to convert evaluation BIOSes to formally releasable BIOSes.

3.6 VGA DEMONSTRATION AND DEBUGGING TOOLS

Chips and Technologies provide a range of debugging and demonstration programs which are available on the TV750 utility disk. Of particular interest is the 535DEBUG program. This is a TSR program which can be invoked at any stage and used to change registers within the 65535 Chip. This is very useful when configuring BIOSes for non-standard displays or applications.

Also present is a MODETEST program, which cycles through various graphics modes, and the 535DEMO suite which describes and demonstrates features of the 65535 chip. These programs are described in more detail on the TV750 Utility disk.

3.7 VGA DISPLAY DRIVER SOFTWARE

Chips and Technologies provide a range of VGA drivers which have been licenced by DSP Design and which are available on the TV750 Utility Disk. The UTILS\DOC directory on the Utility Disk contains information regarding display driver installation for many popular software packages such as Windows, Wordperfect etc.

APPENDIX A: SPECIFICATION

Product:	TV750
Description:	VGA Graphics controller for PC/104 bus.
Memory:	512k or 1 Mbyte memory versions available. 32k byte VGA BIOS EPROM.
Displays:	CRT and flat panel simultaneously. Mono, TFT and STN colour LCDS, EL and plasma displays.
Bus interface:	PC/104 V2.2 16-bit.
Connectors:	Standard PC/104 V2.2 J1 and J2 stackable connectors. Single 50 way right angle VGA output connector.
Dimensions:	Standard PC/104 format. 3.775 in x 3.550 in (PCB), 3.775 in x 3.950 in, with connectors.
Weight:	65g Approx.
Temperature:	0 - 70 degrees C operating
Humidity:	10% - 90% non-condensing.
Power:	+5V / 240mA typical.

APPENDIX B: SETUP CONFIGURATION

The TV750 and TV750-1M are shipped with a simultaneous CRT and flat panel display BIOS (134041.BO2) as standard. The BIOS and jumper E1 are the only configurable parts of the TV750 product.

If the VGA BIOS EPROM is to be fitted on the TV750 (default), then jumper E1 must be fitted in the (2-3) position. If the VGA BIOS is to be combined with the processor BIOS and installed on the processor card then the VGA BIOS EPROM on the TV750 must be removed and jumper E1 fitted in the (1-2) position.

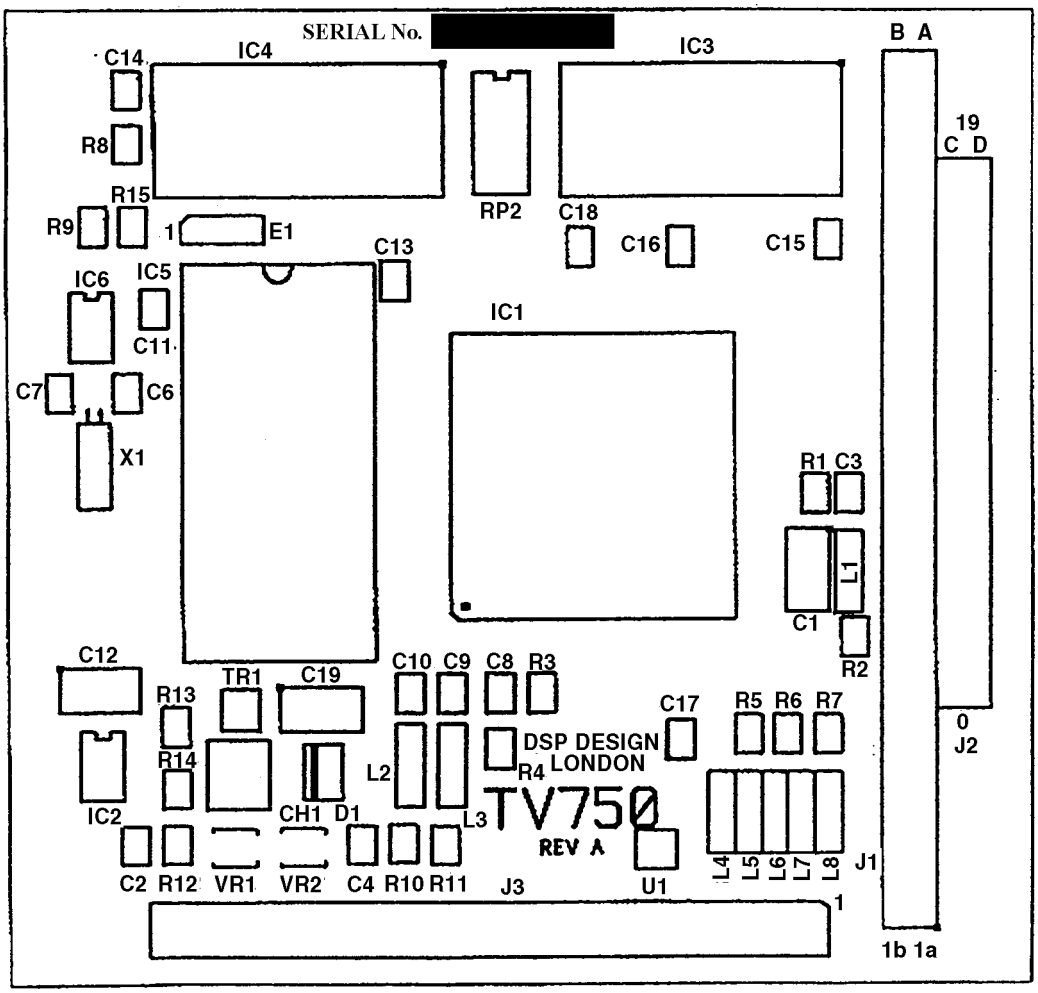
JUMPER E1

1-2 The VGA BIOS EPROM is not fitted to the TV750.
2-3 The VGA BIOS EPROM is installed in IC3 on the TV750.

APPENDIX C: COMPONENT PLACEMENT DIAGRAM

The component placement diagram which follows may be of help in locating components reterred to in this document.

TV750 COMPONENT PLACEMENT DIAGRAM - TOP SIDE



APPENDIX D: CONNECTOR PIN ASSIGNMENTS

There are three connectors on the TV750. J1 and J2 are the PC/104 bus connectors. J3 is a right angled double pin header and all the CRT and LCD signals are present on this connector.

The PC/104 bus connector pin assignments conform to the PC/104 bus specification V2.2. The pin assignment is shown below.

Pin	J1	
	Row A	Row B
0	-	-
1	/IOCHCHK*	0V
2	SD7	RESETDRV*
3	SD6	+5V
4	SD5	IRQ9*
5	SD4	-5V*
6	SD3	DRQ2*
7	SD2	-12V*
8	SD1	/ENDXFR*
9	SD0	+12V*
10	IOCHRDY	(KEY)
11	AEN	/SMEMW
12	SA19	/SMEMR
13	SA18	/IOW
14	SA17	/IOR
15	SA16	/DACK3*
16	SA15	/DRQ3*
17	SA14	/DACK1*
18	SA13	DRQ1*
19	SA12	/REFRESH
20	SA11	SYSCLK*
21	SA10	IRQ7*
22	SA9	IRQ6*
23	SA8	IRQ5*
24	SA7	IRQ4*
25	SA6	IRQ3*
26	SA5	/DACK2*
27	SA4	TC*
29	SA3	BALE
29	SA2	+5V
30	SA1	OSC
31	SA0	0V
32	0V	OV

Pin	J2	
	Row C	Row B
0	0V	0V
1	/SBHE	/MEMCS16
2	LA23	/IOCS16
3	LA22	IRQ10*
4	LA21	IRQ11*
5	LA20	IRQ12*
6	LA19	IRQ15*
7	LA18	IRQ14*
8	LA17	/DACK0*
9	/MEMR*	DREQ0*
10	/MEMW*	/DACK5*
11	SD8	DRQ5*
12	SD9	/DACK6*
13	SD10	DRQ6*
14	SD11	/DACK7*
15	SD12	DRQ7*
16	SD13	+5V
17	SD14	/MASTER*
18	SD15	0V
19	(KEY)	0V

Table 3: PC/104 Pin Assignments

NOTE: These connections are not implemented on the TV750. Pin 1 of J1 connector is marked on the PCB silkscreen with a '1', rows A and B are also marked. J2 pin 0 and Rows C & D are identified in the same way.

J3 Connector Assignment

The J3 connector provides all the signals required to connect the TV750 to a CRT and a flat panel display. The pin assignments are shown below

Pin	Signal	Description	Pin	Signal	Description
2	Red	CRT analog video	1	Gnd	
4	Green	CRT analog video	3	Gnd	
6	Blue	CRT analog video	5	Gnd	
8	Hsync	Horizontal sync	7	Gnd	
10	Vsync	Vertical sync	9	Gnd	
12	Gnd		11	Gnd	
14	/Backlight	Backlight Control[1]	13	Vcc	
16	ENABLEVEE	Vee Control[2]	15	ADJVEE	Adjust Vee[2]
18	ENAVEE	Enable Vee[1]	17	ENAVDD	Enable Panel Vdd[1]
20	P16	P0 to P17 provide 8, 9, 12 or 18 bit data output Refer to table 6 for pin assignment for various panel types	19	P17	P0 to P17 provide 8, 9, 12 or 18 bit data output Refer to table 6 for pin assignment for various panel types
22	P14		21	P15	
24	P12		23	P13	
26	P10		25	P11	
28	P8		27	P9	
30	P6		29	P7	
32	P4		31	P5	
34	P2		33	P3	
36	P0		35	P1	
38	Vcc		37	Vcc	
40	Gnd		39	FLM	First Line Marker
42	Gnd		41	M	ACDCLK
44	Gnd		43	LP	Latch Pulse
46	Gnd		45	SHFCLK	Shift Clock
48	Vcc		47	Vo	Vo Output
50	Vee	Vee Output	49	Gnd	

Table 4: TV750 J3 Pin Assignments

NOTE 1: These pins provide power sequencing control for panel driver electronics. See section 2.7 for more information about power sequencing.

NOTE 2: These signals control the on-board Vee generator. See section 2.6 for more information about the on-board Vee generator

APPENDIX E: DRIVING MONO LCDs WITH THE TV750

The common VGA resolution 640 x 480 monochrome LCDs are almost without exception, dual drive displays with the same set of interface signals and interface timing. Almost all of these displays can be treated as equivalent and interchangeable.

Unfortunately manufacturers differ in the names they give to the interface signals, and they use different connectors. In order to configure a system with a TV750 and mono LCD the user will have to determine which signal on the TV750 to connect to the LCD display. This will involve obtaining a data sheet from the display manufacturer, examining the description of the signals, perhaps refering to the timing diagrams, and then deciding which signal on the TV750 connects to which signal on the LCD.

The TV750 utilities disk contains some VGA BIOSes which have been pre-configured for mono LCDS.

J3		Common Name	Description
Pin No	Name		
36	P0	UD3	Four data lines to drive upper half of display
35	P1	UD2	
34	P2	UD1	
33	P3	UD0	
32	P4	LD3	Four data lines to drive lower half of display
31	P5	LD2	
30	P6	LD1	
29	P7	LD0	
45	SHFCLK	CP2	65535 SHFCLK signal.Clocks data into LCD
41	M	M	65535 ACDCLK signal. Square wave ½ frame frequency. Unused on many LCDs
43	LP	CP1	65535 LP horizontal latch pulse. Latches a line of pixels into LCD
39	FLM	FLM	65535 FLM vertical sync pulses
50	Vee	Vee	-ve voltage for LCD panel. Adjusted with VR1 on TV750
47	Vo	Vo	-ve contrast adjust voltage for LCD. Adjusted with VR2 on TV750
49,46,44	Gnd	Vss	0V (Gnd) suply rail
48,38,37	Vcc	Vdd	+5V supply rail

Table 5: Connection of signals from TV750 to mono LCD

APPENDIX F: DRIVING OTHER FLAT PANELS WITH THE TV750

The table below shows examples of how various types of flat panel display would connect to the TV750. These examples were taken from the Chips and Technologies 65535 data sheet. The TV750 Utility disk contains a number of VGA BIOS configuration files for each of the panels (1-4) shown below.

J3		Signal for			
Pin No	Signal	Panel 1	Panel 2	Panel 3	Panel 4
36	P0	DU7	N/C	B0	UD7
35	P1	DU6	N/C	B1	LD7
34	P2	DU5	B0	B2	UD6
33	P3	DU4	B1	B3	LD6
32	P4	DL7	B2	B4	UD5
31	P5	DL6	N/C	B5	LD5
30	P6	DL5	N/C	G0	UD4
29	P7	DL4	G0	G1	LD4
28	P8	UD3	G1	G2	UD3
27	P9	UD2	G2	G3	LD3
26	P10	UD1	N/C	G4	UD2
25	P11	UD0	N/C	G5	LD2
24	P12	LD3	R0	R0	UD1
23	P13	LD2	R1	R1	LD1
22	P14	LD1	R2	R2	UD0
21	P15	LD0	N/C	R3	LD0
20	P16	N/C	N/C	R4	N/C
19	P17	N/C	N/C	R5	N/C
45	SHFCLK	XCK	NCLK	CK	CL2
43	LP	LP	N/C	HSYNC	CL1
41	M	N/C	N/C	N/C	M
39	FLM	YD	N/C	VSYNC	FLM
50	VEE	VEE	N/C	N/C	VEE
38	VCC	VDD	VDD	VCC	VDD
40	Gnd	VSS	Gnd	Gnd	VSS

Table 6: Example LCD Panel Interface

PANEL 1: Sharp LM64C08P (640x480 Colour STN-DD LCD panel).
Use the STNDD.BMS file from the TVUTILS Utility disk.

PANEL2: Toshiba LTM09C015-1 (640x480 512 Colour TFT LCD panel).
Use the TFTCLIDR.BMS file from the TVUTILS Utility Disk.

PANEL3: Sharp LQ10D311 (640x480 256k colour TFT LCD panel).
Use the 18BTFT.BMS file from the TVUTILS Utility Disk.

PANEL 4: Sanyo LCM5327-24NAK (640x480 colour STN LCD panel).
Use the STN4BIT.BMS file from the TVUTILS Utility Disk.

APPENDIX G: TV750 OPTIONS AND ORDERING INFORMATION

The TV750 high performance VGA graphics module is available with 512K or 1M byte of DRAM. The TV750 comes with 512k of video memory and the TV750-1M comes with 1M byte of video memory. Options and other PC/104 accessories are detailed below.

ORDER CODES

TV750	High performance VGA graphics module with 512k of video memory installed as standard
TV750-1M	High performance VGA graphics module with 1M byte of Video memory installed as standard

ACCESSORIES - The following part numbers should be used to order various accessories:

TV750-CRTCAB Cable to connect the TV750 to a standard 15 pin VGA monitor

VGA-14	VGA colour monitor
LCD480	640 x 480 Mono VGA LCD display
TVUTILS	Utilities disk for the TV750
TCDEV	PC/104 development platform
TCPSU	Power supply unit for the TCDEV
TCDOS	Microsoft MS-DOS Operating System
TCUTILS	Utilitys disk containing software for all DSP PC/104 products except the TV750 and TV750-1M
TRM-TC	Collection of PC/104 Technical Reference Manuals
TCPAK	Contains a TCDEV, TCPSU, TCUTILS and TRM-TC in one starter pack

DSP Design have designed a number of PC/104 boards specifically for the PC/104 bus. For details of these boards see the latest copy of our TC product data sheets.

APPENDIX H: FAULT REPORTING

DSP Design mlakes every effort to ship products and documentation which are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a “Product Fault Report" form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form to your supplier.

Prior to returning a faulty product, please check the following:

1 The board has been correctly configured for the intended application (see earlier appendix for board installation details).

2. The power supplies are providing correct voltage levels.

3. Cabling to the board is sound and connected correctly.

4. Other cards in the system are known to be correctly configured and functioning.

5. **PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

Your help with this will enable us to sort out your problem more quickly. Thank you.

PRODUCT FAULT REPORT

CUSTOMER INFORMATION
COMPANY NAME:
INDIVIDUAL CONTACT:
PHONE NO:

PRODUCT INFORMATION
PRODUCT/DOCUMENT:
SERIAL NO:
DATE OF RETURN:

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

IN WHAT CONFIGURATION IS THE BOARD USUALLY USED? (WHAT OTHER BOARDS, WHAT SOFTWARE ETC)?

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT:

REPAIRED BY:

CHARGES TO BE INVOICED: E

DATE OF RETURN:

RETURNED BY: