# TS400
# Four Channel Serial
# Communications Board

## V1.1a
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Whilst every effort has been made to ensure that this document is correct, errors can occur. If you find any errors or omissions please let us know, so that we can put this right.



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## INTRODUCTION

This document provides the specification for a four channel serial communications card for the PC/104 bus.

The TS400 provides four PC compatible asynchronous serial ports, each of which can be configured for RS-232 or RS-485 operation.

Addresses and interrupts are jumper selectable, and more than one TS400 can be used in any PC/104 system.

The card is based on the Startech ST1 6C554 or Texas Instruments TLI 6C554 chip. This chip contains four UARTs (Universal Aysnchronous Receiver/Transmitter). These UARTs are improved versions of the NS16C550, which includes transmit and receive FIFO buffers.

Powerful interrupt driven driver software is available for the board. Contact your supplier for details.

Key features:

- **16C550-type UARTS, for PC compatibility.**
- **RS-232 provided as standard. All eight signals found on PC serial ports are provided. In RS-232 mode the maximum data rate is 115.2k baud.**
- **RS-485 transceivers can be installed by the user on each channel individually. Both half duplex (single twisted pair) and full duplex (two twisted pair) operation is possible. In RS485 mode the maximum data rate is 460.8k baud.**
- **Optional RS-485 termination networks are provided on-board.**
- **The PC/104 interface is an 8-bit I/O mapped interface. Addresses are jumper selectable at a range of standard and non-standard I/O addresses.**
- **Jumpers allow each UART to be connected to its own PC/104 IRQ interrupt line, or all four interrupts can share a single IRQ line.**
- **A range of driver software (provided by National Semiconductor) is provided.**
- **Low power, +5V only operation.**
- **A shutdown pin can reduce power consumption further.**
- **Complies with PC/104 specification Revision 2.2.**


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**·PC/104 INTERFACE**

The ST16C554 Quad UART chip which is used on theTS400, is software compatible with standard PC serial ports. This PC compatibility therefore defines the TS400's interface to the PC/104 bus.

The UART functions use an 8-bit PC/104 interface and are I/O mapped at one of a number of pre-determined addresses (jumper selectable). One of eight interrupts can be selected by each UART (jumper selectable). DMA is not required, and nor is memory space.

## 2.1 I/O ADDRESSES

Each UART on the TS400 occupies 8 bytes of the PC/104 I/O space. A address decoder GAL device is pre-programmed with a number of standard and non-standard serial port addresses. These addresses are selected by jumpers. Appendix B describes how to set these addresses.

Users should check the other boards in their PC/104 system and select addressess and interrupt options which do not conflict with other boards.

The address decoder decodes 10 I/O address pins (A0-A9). Thus the TS400 is aliased within the 16-bit (64k byte) I/O address space of the Intel processor. For example, the COM1: I/O address (3F8h) will also appear at I/O addresses 7F8h, BF8h, 13F8h, 17F8h and so forth.

The set of "standard" addresses provided allows the TS400 to be configured as COM1: to COM4:. For systems which already have serial ports on the processor card, further address options allow for the TS400 ports to begin at COM2:, COM3: COM4:, COM5: or COM6:, thus allowing the TS400 to avoid the COM1:, COM2:, COM3:, COM4: or COM5: serial ports elsewhere in the system, or for two TS400s to be used in any one system.

The "standard" serial port addresses do not form a contiguous block of 32 successive addresses. Also, since in general only the first four serial port addresses (COM1: - COM4:) are by defined as defacto standards, DSP Design have allocated new previously unused addresses to the further serial ports (COM5: - COM9:). The addresses for the "standard" serial ports are given in Table 1.

| Port | Address Range | Standard Interrupt |
|---|---|---|
| Com1: | 3F8h - 3FFh | IRQ4 |
| Com2: | 2F8h - 2FFh | IRQ3 |
| Com3: | 3E8h - 3EFh | IRQ4 |
| Com5: | 2E8h - 2EFh | IRQ3 |
| Com5: | 338h - 33Fh | See Section 2.2 for information regarding interrupts |
| Com6: | 238h - 23Fh | |
| Com7: | 380h - 387h | |
| Com8: | 280h - 287h | |
| Com9: | 3A0h - 3A7h | |

Table 1: 'standard" PC Serial Port Addresses

In addition to these standard serial port addresses, the TS400 address decoder can also assign other, non-standard, serial port addresses to the TS400. These non-standard options result in the TS400 occupying 32 contiguous addresses, with each of the four UARTs occupying eight addresses.

Table 2 lists the addresses occupied in the non-standard address mode. These seven sets of addresses have been chosen to avoid, for the most part, addresses used by standard PC peripherals.

| Address Range | CSA Address | CSB Address | CSC Address | CSD Address |
|---|---|---|---|---|
| 220 - 23F | 220 - 227 | 228 - 22F | 230 - 237 | 238 23F |
| 240 - 25F | 240 - 247 | 248 - 24F | 250 - 257 | 258 - 25F |
| 280 - 29F | 280 - 287 | 288 - 28F | 290 - 297 | 298 - 29F |
| 300 - 31F | 300 - 307 | 308 - 30F | 310 - 317 | 318 - 31F |
| 320 - 33F | 320 - 327 | 328 - 32F | 330 - 337 | 338 - 33F |
| 340 - 35F | 340 - 347 | 348 - 34F | 350 - 357 | 358 - 35F |
| 380 - 39F | 380 - 387 | 388 - 38F | 390 - 397 | 398 - 39F |

Table 2: Non-Standard Serial Port Addresses

Since the I/O address decoding is done within a GAL programmable logic chip, in the unlikely event that these address options are insufficient DSP Design would be able to design another GAL with different addresses. There would be an additional engineering charge for this.

## 2.2 INTERRUPT SELECTION

Each of the four UARTs on the TS400 has its own interrupt pin. These pins can be routed to PC/104 IRQ interrupt request signals, through jumper area E2.

The interrupt can be selected from one of the following.

| Interrupts Available |
|---|
| IRQ3 |
| IRQ4 |
| IRQ5 |
| IRQ9 (IRQ2) |
| IRQ10 |
| IRQ11 |
| IRQ14 |
| IRQ15 |

In a system with more than one TS400, users will quickly begin to run out of IRQ signals, if each UART used a separate IRQ signal. For this reason the TS400 features an option for ORing all four interrupts and sending the OR-ed interrupt to a single PC/104 IRQ signal. This mode of operation requires the interrupt-driven software to interrogate each of the UARTs in turn, to determine which is asserting the IRO line. Driver software for this mode of operation is available from your supplier.

Appendix B describes how to configure the interrupts.

Users should check the other boards in their PC/104 system and select address and interrupt options which do not conflict with other boards.

## 3 UARTS AND BAUD RATE GENERATION

The TS400 board is based on the Startech ST16C554 or Texas Instruments TL16C554 chip. This chip contains four UARTs (Universal Aysnchronous Receiver/Transmifter). These UARTs are improved versions of the NS16C550, which includes transmit and receive FIFO buffers. These FIFOs result in higher overall throughput, since interrupt service routines have longer to respond to an interrupt before a data underrun or overrun occurs.

A data sheet of the ST16C554 is included in Appendix D.

Each of the four UARTs include a separate baud rate generator. In normal operation a crystal oscillator circuit provides a 1.8432MHz clock for the baud rate generator. This is divided internally by a 16-bit programmable counter to set the required baud rate. The minimum divisor value (1) gives the maxiumum baud rate of 115.2k baud. The standard 1.8432MHz clock frequency allows standard PC software to select standard PC baud rates.

Note that 115.2k baud is the highest baud rate used in PC compatible serial ports. The RS232 transceivers used on the TS400 will operate at this high baud rate.

The 1.8432MHz clock signal is derived from a 7.373MHz crystal, which is divided by four. However, solder links allow the original 7.373MHz clock, and a 3.686MHz clock, to be routed to the ST16C554. While these other two clock signals will clearly produce non-standard baud rates with standard software, they have been provided particularly for RS-485 transmission, since RS-485 transceivers support higher baud rates.

It would also be possible to fit a different frequency crystal, for non-standard baud rates. DSP Design would impose a minimum-order quantity for none standard configurations.

## 4 RS-232 AND RS-485 TRANSCEIVERS

The TS400 serial ports can be buffered by RS-232 transceivers or RS-485 transceivers. Each port can be configured individually. The RS-232 signals are available on connector J4 and the RS-485 signals on connector J3.

### 4.1 RS-232 TRANSCEIVERS

The RS-232 transceivers buffer three output signals and five inputs. The outputs from the TS400 are TxD (Transmit Data), RTS (Request to Send) and DTR (Data Terminal Ready). The inputs to the TS400 are RxD (Receive Data), CTS (Clear to Send), DSR (Data Set Ready), DCD (Data Carrier Detect) and RI (Ring Indicator).

The RS-232 transceiver chip features protection against ESD (electrostatic discharge) damage.

The RS-232 signals are taken to the outside world through connector J4. This is a 40-way IDC connector, and the ports are arranged as four sets of 10 pins. The assignment of the signals within each group of 10 signals has been designed to directly connect the cable to the 9-pin male D-type connectors, which are used on most PCs. Appendix A gives the pin assignments for this connector.

In normal operation the RS-232 transceiver chip is permanently on. There are solder link options to reduce the power consumption under hardware or software control. The setting of this link is described in Appendix B.

One of the power-down options requires the SHDN- signal to be asserted to put the RS-232 transceivers into a low power state. In the low power state both the inputs and outputs of the RS-232 transceivers go to a high impedance state, and the baud rate generator oscilator is shut down.

The other link-selectable power-down option is to use the DTR signal. In this mode, when the DTR signal is asserted (true, on) the transceiver operates normally. When it is off the RS-232 transceiver goes into a low power mode, with all the outputs and four of the five inputs in a high impedance state. The RI (Ring Indicator) input still operates, and can be used to generate an interrupt to wake up a powered down system.

When a channel is configured for RS-485 operation a solder link must be changed to disable the RS-232 transceiver chip.

**4.2 RS-485 TRANSCEIVERS**

RS-485 transceiver chips can be fitted by the user into sockets on the TS400, to implement full duplex or half duplex RS-485 serial ports.

The RS-485 transceivers drive balanced twisted pair cables. Each end of the cable is typically terminated in the characteristic impedance of the cable. The balanced twisted pair operation allows better noise immunity, longer cable runs and higher data rates than RS-232.

RS-485 supports multidrop operation, where several RS-485 nodes connect to a single twisted pair. Software running on each of the nodes must agree a protocol which ensures that only one node drives the cable at a time.

In half duplex operation a single twisted pair is used, with each node alternately transmitting and receiving on the same twisted pair. On the TS400 the direction is controlled by the RTS signal.

Full duplex mode is for point to point operation, with one twisted pair for transmission and another for reception.

On the TS400 RS-485 is implemented as follows.

For half duplex operation one MAX485 transceiver chip is installed in the appropriate socket. When the RTS signal is off (not asserted) the transmitter in the RS-485 transceiver chip is off, and thus the TS400 is in receive mode. Incoming data will be sent to the UART RxD pin. When the RTS signal is on (asserted) the transmitter in the RS-485 transceiver chip is on, and thus the TS400 is in transmit mode. The TS400 can be configured so that either the receiver receives the data which is being transmitted, or that it does not.

For full duplex operation two MAX485 transceiver chipsare installed into the appropriate sockets. One chip is attached to the transmit twisted pair and the other chip is attached to the receive twisted pair. When the RTS signal is off (not asserted) the transmitter is off. When the RTS signal is on (asserted) the transmitter is on, and thus the TS400 is able to transmit. In full duplex mode the TS400 always receives data from the receive twisted pair.

Appendix B describes configuring the TS400 for the various RS-485 modes.

There are separate termination networks for the transmit and receive twisted pairs. These networks are available at pins on the J5 socket, and if the termination function is required then the termination network pins can be connected to the adjacent data twisted pair pin. The termination network consists of two parts.

The transmission line termination is provided by a 120 ohm resistor, in series with a l00nF capacitor, connected between the two pins of the twisted pair. This terminates the transmission line with an impedance close to that of the twisted pair, reducing reflection and thus ringing on the line. The series capacitor ensures that no DC current is drawn, reducing power consumption.

There are also pull-up and pull-down resistors which provide a small DC bias on the twisted pair, ensuring that when no node is driving, the twisted pair receivers will see a mark rather than a space. The resitors are both 10k ohms. The pull-up resistor is connected to VCC (+5V) and the pull-down resistor is connected to GND.

The RS-485 signals are taken to the outside world through connector J3. This is a 50-way connector, and the ports are arranged as four sets of 12 pins. Of these 12 pins six are used for full duplex operation, and transmission in full-duplex mode. The other six signals are used for receive data in full duplex mode. Appendix A gives pin assignments of this connector.

## 5 SOFTWARE

The serial ports are PC compatible, and thus any comms drivers or libraries which operate with PC serial ports should work with the TS400.

DSP Design have selected a driver package which will work with the TS400. It will also work with other PC compatible serial ports, for example DSP Designs range of processor cards.

The package is called COMM-DRV and is available under a licence agreement. A separate manual is available for this serial comms package and is called TRM-COMMDRV.

The package works with MS-DOS and Windows. It is an interrupt driven driver, which supports multiple interrupts on a single IRQ signal. It provides a high degree of user control of the serial ports.

The package includes the following elements:

- **An MS-DOS device driver which is loaded from the CONFIG.SYS file, and which allows the serial port to be addressed as a standard file.**
- **A form of a TSR (Terminate and Stay Resident) program which is loaded from the command line. This implements an extended INT14 interface, and a FOSSIL interface.**
- **A serial Comms monitor.**
- **A TSR which redirects incoming serial data to the keyboard buffer.**
- **A custom file transfer utility.**
- **An XMODEM/YMODEM/ZMODEM file transfer program.**
- **A dumb terminal emulator.**
- **An installation program.**

## 6 SERIAL COMMS - A BASIC TUTORIAL

This section is intended to provide an insight into the basics of serial communications.

Serial communication is basically the conversion of a 5 to 8 bit data byte to a stream of digital data and back again. In effect, a byte may be transmitted as its binary equivalent over a single wire or received over a single wire. The advantage of this method of transmission is that less wires are required to transmit data which means that this method of communication is much cheaper and simpler than transmitting the data one full byte at a time. It is the responsibility of the UART (Universal Asynchronous Receiver Transmitter) to take the 5-8 bit byte and convert it to a serial data stream and back again.

At any given time the signal on a serial line (wire) is either at a positive voltage (logical 1), also known as the MARK state, or at a negative voltage (logical 0), also known as the SPACE state. Before the first bit of any byte is sent, the signal drops to a logical 0 to indicate the start of a stream of data. This logical zero at the start of the stream is called the START BIT. Following this START BIT the signal fluctuates between logical 0 and logical 1 depending on the character being transmitted. At the end of the transmission of the character, the signal returns to the MARK state. The MARK state immediately after the transmission of a stream of data is called a STOP BIT.

At this point you may want to know what is the duration of a bit. In other words, how long does the signal stay in a particular state to define a bit. The answer is simple. It is dependent on the baud rate. The baud rate is the number of times the signal can switch states in one second. Therefore, if the line is operating at 9600 baud, the line can switch states 9,600 times per second. This means each bit has the duration of 1/9600 of a second or about 104.17 usecs.

When transmitting a character there are other characteristics other than the baud rate that must be known or that must be setup. The characteristics define the entire interpretation of the data stream.

The first characteristic is the length of the byte that will be transmitted. This length in general can be anywhere from 5 to 8 bits.

The second characteristic is partity. The partity characteristic can be even, odd, mark, space, or none. If even parity, then the last data bit transmitted will be a logical 1 if the data transmitted had an odd amount of 1 bits. If odd parity, then that last data bit transmitted will be a logical 1 if the data transmitted had an even amount of 1 bits. If mark parity, then the last transmitted data bit will always be a logical 1. If space parity, then the last transmitted data bit will always be a logical 0. If no parity then there is no parity bit transmitted.

The third characteristic is the amount of stopbits. This value in general is 1, 1.5, or 2.

Assuming we wanted to send ‘A’ over the serial port. The binary representation of the letter ‘A’ is 01000001. Remembering that bits are transmitted from least significant bit (LSB) to most significant bit (MSB), the bit stream transmitted would be as follows for the line characteristics 8 bits, no parity, 1 stop bit, 9600 baud.

**LSB** (1 1 0 0 0 0 0 1 0 0) **MSB**

The above represents

(Start Bit)(Data Bits)(Stop Bit)

To calculate the actual byte transfer rate simply divide the baud rate by the number of bits that must be transferred to each byte of data. In the case of the above example, each character requires 10 bits to be transmitted for each character. As such, at 9600 baud, up to 960 bytes can be transferred in one second.

The above discussion was concerned with the "electrical/logical" characteristics- of the data stream. We will expand the discussion to line protocol.

Serial communication can be half duplex or full duplex. Full duplex communication means that a device can receive and transmit data at the same time. Half duplex means that the device cannot send and receive at the same time. It can do them both, but not at the same time. Half duplex communication is all but outdated except for a very small focused set of applications.

Half duplex communication needs at a minimum two wires, signal ground and the data line. Full duplex communication needs at a minimum three wires, signal ground, transmit data line, and receive data line. The RS232 specification governs the physical and electrical characteristics of serial communications. This specification defines several additional signals that are asserted (set to logical 1) for information and control beyond the data signals and signal ground.

These signals are the Carrier Detect Signal (CD), asserted by modems to signal a successful connection to another modem, Ring Indicator (RI), asserted by modems to signal the phone ringing, Data Set Ready (DSR), asserted by modems to show their presence, Clear To Send (CTS), asserted by modems if they can receive data, Data Terminal Ready (DTR), asserted by terminals to show their presence, Request To Send (RTS), asserted by terminals if they can receive data.

The above paragraph eluded to hardware flow control. Hardware flow control is a method that two connected devices use to tell each other electronically when to send or when not to send data. A modem in general drops (logical 0) its CTS line when it can no longer receive characters. It re-asserts it when it can receive again. A terminal does the same thing instead withe the RTS signal. Another method of hardware flow control in practice is to perform the same procedure in the previous paragraph except that the DSR and DTR signals are used for the handshake.

Note that hardware flow control requires the use of additional wires. The benefit to this however is crisp and reliable flow control. Another method of flow control used is known as software flow control. This method requires a simple 3 wire serial communication link, transmit data, receive data, and signal ground. If using this method, when a device can no longer receive, it will transmit a character that the two devices agreed on. This character is known as the XOFF character. This character is generally a hexadecimal 13. When a device can receive again it transmits an XON character that both devices ageed to. This character is generally a hexadecimal 11.

The COMM-DRV serial communications software (see section 5 SOFTWARE), has the ability to perform all the above mentioned flow control protocols internally, and without user intervention.

There is a special line condition that should be mentioned here. Whenever the transmit signal remains in the SPACE state for more than the time it takes to transmit a character, it is called a BREAK. This is usually used to get the attention of another device.

**RS232 CABLING**

The RS232 protocol is one of the most common PC serial port configurations. The cables and connectors used are fairly standard and are described below.

Serial devices are shipped in two basic configurations. These are DCE (Data Communications Equipment) or DTE (Data Terminal Equipment). Devices such as terminals are considered DTE(s), while device like modems are considered DCE(s). When connecting devices using straight through cables (Pin for Pin connections), it is assumed that one device is a DCE and the other a DTE. If both devices are DTEs or DCEs, then a null modem is needed between the two devices. A null modem re-maps a number of pins as described in table4 below.

Most PC serial ports or multipart cards are shipped assuming that they will be connected to a modem (DCE).

| Pin | Signal | Name |
|---|---|---|
| 1 | NC | Chassis Ground |
| 2 | TXD | Transmit data |
| 3 | RXD | Receive Data |
| 4 | RTS | Request to Send |
| 5 | CTS | Clear to Send |
| 6 | DSR | Data Set ready |
| 7 | GND | Signal Ground |
| 8 | DCD | Data Carrier Detect |
| 20 | DTR | Data Terminal Ready |
| 22 | RI | Ring Indicator |

Table 3: RS-232 25 way D-Type Serial Port Connections

| Pin | Signal | Name |
|---|---|---|
| 1 | DCD | Data Carrier Detect |
| 2 | TXD | Transmit data |
| 3 | RXD | Receive Data |
| 4 | DTR | Data Terminal Ready |
| 5 | GND | Signal Ground |
| 6 | DSR | Data Set ready |
| 7 | RTS | Request to Send |
| 8 | CTS | Clear to Send |
| 9 | RI | Ring Indicator |

Table 4: RS-232 9 way D-Type Serial Port Connections

A null modem cable can be connected between two DTE or DCE devices. The null modem cable essentially swaps the necessary signals to enable communication between the two items of DTE or DCE equipment. For example, in the table below connector A could refer to one DTE device cable and connector B refer to the other DTE device cable. Alternativley both devices could be DCE equipment.

| Connector A | | Connector B | |
|---|---|---|---|
| Signal | Pin | Pin | Signal |
| TXD | 2 | 3 | RXD |
| RXD | 3 | 2 | TXD |
| RTS | 4 | 5 | CTS |
| CTS | 5 | 4 | RTS |
| DSR | 6 | 20 | DTR |
| DTR | 20 | 6 | DSR |

Table 5: RS-232 Null Modem Cable Connections

## APPENDIX A - PIN ASSIGNMENTS

There are five connectors on the TS400. Connectors J1 and J2 are defined by the PC/104 specification, and are in effect the PC/AT bus signals.

### A.1 PC Bus Connector (J1)

The PC bus connector is, for the most part, what it sounds - the signals found on PC bus expansion cards.

The PC bus connector is labeled J1 - it is the 64-way connector on the TS400. It is defined by the PC/104 specification. The connector has two parts - male and female - so that the TS400 can be stacked in a PC/104 board stack. The PC bus connector is used as the main set of signals between the TS400 and additional I/O boards, as well as being part of the mechanical system which secures the TS400 processor to other PC/104 boards.

PC bus cards have 62 pins - rows a and b, and pins 1 to 31. The PC/104 boards have most of these signals present on the connector marked J1, as well as two extra pins. The two extra pins (32a and 32b) are two additional GND pins (the 0V power supply signal).

Table A1 lists the pin assignments of the PC bus connector, J1.

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1a | /IOCHCHK * | 1b | 0V (Gnd) |
| 2a | SD7 | 2b | RESETDRV |
| 3a | SD6 | 3b | +5V (VCC) |
| 4a | SD5 | 4b | IRQ2/9 |
| 5a | SD4 | 5b | -5V * |
| 6a | SD3 | 6b | DRQ2 * |
| 7a | SD2 | 7b | -12V* |
| 8a | SD1 | 8b | /ENDXFR * |
| 9a | SD0 | 9b | +12V * |
| 10a | IOCHRDY * | 10b | (KEY) |
| 11a | AEN * | 11b | /SMEMW * |
| 12a | SA19 * | 12b | /SMEMR * |
| 13a | SA18 * | 13b | /IOW |
| 14a | SA17 * | 14b | /IOR |
| 15a | SA16 * | 15b | /DACK3 * |
| 16a | SA15 * | 16b | DRQ3 * |
| 17a | SA14 | 17b | /DACK1 * |
| 18a | SA13 | 18b | DRQ1 * |
| 19a | SA12 | 19b | /REFRESH * |
| 20a | SA11 | 20b | CLK * |
| 21a | SA10 | 21b | IRQ7 * |
| 22a | SA9 | 22b | IRQ6 * |
| 23a | SA8 | 23b | IRQ5 |
| 24a | SA7 | 24b | IRQ4 |
| 25a | SA6 | 25b | IRQ3 |
| 26a | SA5 | 26b | /DACK2 * |
| 27a | SA4 | 27b | TC * |
| 28a | SA3 | 28b | BALE * |
| 29a | SA2 | 29b | +5V (VCC) |
| 30a | SA1 | 30b | OSC * |
| 31a | SA0 | 31b | 0V (Gnd) |
| 32a | 0V (Gnd) | 32b | 0V (Gnd) |

Table A1: TS400 PC Bus Connector (J1) Pin assignments
* These signals are not used on TS400

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### A.2 AT BUS EXTENSION CONNECTOR (J2)

The J2 connector is defined by the PC/104 specification. It carries the signals required for 16-bit bus cycles, as used on AT expansion boards. On the TS400 it is only used for interrupt and power connections.

The connector has two parts - male and female - so that the TS400 can be stacked in a PC/104 board stack. The AT bus connector is used to provide 16-bit data transfers, as well as being part of the mechanical system which secures the TS400 processor to other PC/104 boards.

PC bus cards have 36 pins - rows c and d, and pins 1 to 18. The PC/104 boards have most of these signals present on the connector marked J2, as well as four extra pins. Three of the extra pins (0c, Od and 19d) are additional GND pins (the OV power supply signal). The other extra pin (19c) is a key position.

The pin assignments of J2 are given in Table A2:

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 0c | 0V (Gnd) | 0d | 0V (Gnd) |
| 1c | /SBHE * | 1d | /MEMCS16 * |
| 2c | LA23 * | 2d | /IOCS16 * |
| 3c | LA22 * | 3d | IRQ10 |
| 4c | LA21 * | 4d | IRQ11 |
| 5c | LA20 * | 5d | IRQ12 * |
| 6c | LA19 * | 6d | IRQ15 |
| 7c | LA18 * | 7d | IRQ14 |
| 8c | LA17 * | 8d | /DACK0 * |
| 9c | /MEMR * | 9d | DRQ0 * |
| 10c | /MEMW * | 10d | /DACK5 * |
| 11c | SD8 * | 11d | DRQ5 * |
| 12c | SD9 * | 12d | /DACK6 * |
| 13c | SD10 * | 13d | DRQ6 * |
| 14c | SD11 * | 14d | /DACK7 * |
| 15c | SD12 * | 15d | DRQ7 * |
| 16c | SD13 * | 16d | +5V (VCC) |
| 17c | SD14 * | 17d | /MASTER * |
| 18c | SD15 * | 18d | 0V (Gnd) |
| 19c | (KEY) | 19d | 0V (Gnd) |

Table A2: TS400 AT BUS Connector (J2) Pin Assignments
* These signals are not used on the TPS400

### A.3 RS-485 INTERFACE CONNECTOR (J3)

The J3 connector carries the RS-485 signals. The connector is divided into four groups of twelve signals, one for each of the four UARTS, plus two other pins - the power down signals and a 'not connect'pin.

Within each UART's twelve pins are two groups of six pins - one for the twisted pair used for half duplex operation and for transmit in full-duplex operation, and the other for the twisted pair used for receiving in full-duplex operation. As an example, on channel A TXA+ and TXA- are the half-duplex pair and the full-duplex transmit pair, and RXA+ and RXA- are the full-duplex receive pair. Of each group of six pins, two are the twisted pair itself, two are for the termination network, and there is one each for VCC and GND power pins.

If the termination network is required then the termination network pin should be tied to the adjacent twisted pair pin. For example, to add termination to channel D, tie TTXD+ to TXD+, and TTXD- to TXD-.

The pin assignments of J3 are given in Table A3.

| Function | Name | Pin | Channel | Pin | Name | Function |
|---|---|---|---|---|---|---|
| Power | VCC | 1 | D | 2 | TTXD+ | Terminator |
| Data (Tx) | TXD+ | 3 | | 4 | TXD- | Data (Tx) |
| Terminator | TTXD- | 5 | | 6 | GND | Power |
| Power | VCC | 7 | | 8 | TRXD+ | Terminator |
| Data (Rx) | RXD+ | 9 | | 10 | RXD- | Data (Rx) |
| Terminator | TRXD- | 11 | | 12 | GND | Power |
| Power | VCC | 13 | C | 14 | TTXC+ | Terminator |
| Data (Tx) | TXC+ | 15 | | 16 | TXC- | Data (Tx) |
| Terminator | TTXC- | 17 | | 18 | GND | Power |
| Power | VCC | 19 | | 20 | TRXC+ | Terminator |
| Data (Rx) | RXC+ | 21 | | 22 | RXC- | Data (Rx) |
| Terminator | TRXC- | 23 | | 24 | GND | Power |
| Power | VCC | 25 | B | 26 | TTXB+ | Terminator |
| Data (Tx) | TXB+ | 27 | | 28 | TXB- | Data (Tx) |
| Terminator | TTXB- | 29 | | 30 | GND | Power |
| Power | VCC | 31 | | 32 | TRXB+ | Terminator |
| Data (Rx) | RXB+ | 33 | | 34 | RXB- | Data (Rx) |
| Terminator | TRXB- | 35 | | 36 | GND | Power |
| Power | VCC | 37 | A | 38 | TTXA+ | Terminator |
| Data (Tx) | TXA+ | 39 | | 40 | TXA- | Data (Tx) |
| Terminator | TTXA- | 41 | | 42 | GND | Power |
| Power | VCC | 43 | | 44 | TRXA+ | Terminator |
| Data (Rx) | RXA+ | 45 | | 46 | RXA- | Data (Rx) |
| Terminator | TRXA- | 47 | | 48 | GND | Power |
| Shut Down | SHDN | 49 | | 50 | N/C | |

Table A3: TS400 RS-485 Connector (J3) Pin assignments

### A.4 RS-232 INTERFACE CONNECTOR (J4)

The J4 connector carries the RS-232 signals. The connector is divided into four groups of ten signals, one for each of the four UARTS.

The ten pins corresponding to each channel are arranged so that they can be directly connected to a 9-way male D-type connector. If this is done then the D-type pin assignments will comply with the defacto pin assignments used on PCs. Table A4 gives the D-type connector pin numbers in the columns marked D-Type.

The pin assignments of J3 are given in Table A4:

| D-Type | Name | Pin | Channel | Pin | Name | D-Type |
|---|---|---|---|---|---|---|
| 1 | DCD | 1 | | 2 | DSR | 6 |
| 2 | RXD | 3 | | 4 | RTS | 7 |
| 3 | TXD | 5 | A | 6 | CTS | 8 |
| 4 | DTR | 7 | | 8 | RI | 9 |
| 5 | GND | 9 | | 10 | VCC | |
| 1 | DCD | 11 | | 12 | DSR | 6 |
| 2 | RXD | 13 | | 14 | RTS | 7 |
| 3 | TXD | 15 | B | 16 | CTS | 8 |
| 4 | DTR | 17 | | 18 | RI | 9 |
| 5 | GND | 19 | | 20 | VCC | |
| 1 | DCD | 21 | | 22 | DSR | 6 |
| 2 | RXD | 23 | | 24 | RTS | 7 |
| 3 | TXD | 25 | C | 26 | CTS | 8 |
| 4 | DTR | 27 | | 28 | RI | 9 |
| 5 | GND | 29 | | 30 | VCC | |
| 1 | DCD | 31 | | 32 | DSR | 6 |
| 2 | RXD | 33 | | 34 | RTS | 7 |
| 3 | TXD | 35 | D | 36 | CTS | 8 |
| 4 | DTR | 37 | | 38 | RI | 9 |
| 5 | GND | 39 | | 40 | VCC | |

Table A4: TS400 RS-232Connector (J4) Pin assignments

# APPENDIX B - CONFIGURATION

There are two jumper areas and 15 solder link areas on theTS400, which may need to be configured by the user.

The two jumper areas select the I/O addresses and the interrupts. The solder link areas are less likely to be changed, and are concerned mostly with configuring the transceiver chips.

The default settings, when the TS400 leaves the factory, are indicated in each section below.

## B.1 ADDRESS SELECTION - JUMPER AREA E1

Jumper area E1 selects the addresses at which the TS400 UARTs appear. There are “standard” address options and non-standard address options, as described in section 2.1. In Table B1 below the “standard” addresses are listed as COM1, COM2 etc, and the non-standard addresses are given as hex numbers. Table B.2 provides the actual addresses of the “standard” addresses, COM1, COM2 etc.

Note that you must not place a jumper in row 1 of E1.

| E1 | | | | | Channell | | | |
|---|---|---|---|---|---|---|---|---|
| Row 6 | Row 5 | Row 4 | Row 3 | Row 2 | A | B | C | D |
| A - B | A - B | A - B | A - B | A - B | | | | |
| A - B | A - B | A - B | A - B | B - C | 380 - 387 | 388 - 38F | 390 - 397 | 398 - 39F |
| A - B | A - B | A - B | B - C | A - B | 340 - 347 | 348 - 34F | 350 - 357 | 358 - 35F |
| A - B | A - B | A - B | B - C | B - C | 320 - 327 | 328 - 32F | 330 - 337 | 338 - 33F |
| A - B | A - B | B - C | A - B | A - B | 300 - 307 | 308 - 30F | 310 - 317 | 318 - 31F |
| A - B | A - B | B - C | A - B | B - C | 280 - 287 | 288 - 28F | 290 - 297 | 298 - 29F |
| A - B | A - B | B - C | B - C | A - B | 240 - 247 | 248 - 24F | 250 - 257 | 258 - 25F |
| A - B | A - B | B - C | B - C | B - C | 220 - 227 | 228 - 22F | 230 - 237 | 238 - 23F |
| A - B | B - C | A - B | A - B | X | | | | |
| A - B | B - C | A - B | B - C | A - B | COM6 | COM7 | COM8 | COM9 |
| A - B | B - C | A - B | B - C | B - C | COM5 | COM6 | COM7 | COM8 |
| A - B | B - C | B - C | A - B | A - B | COM4 | COM5 | COM6 | COM7 |
| A - B * | B - C * | B - C * | A - B * | B - C * | COM3 * | COM4 * | COM5 * | COM6 * |
| A - B | B - C | B - C | B - C | A - B | COM2 | COM3 | COM4 | COM5 |
| A - B | B - C | B - C | B - C | B - C | COM1 | COM2 | COM3 | COM4 |
| B - C | X | X | X | X | | | | |

Table B1: Jumper E1 Settings - Address Selection
* Default Setting

| Port | Address Range |
|---|---|
| COM1 | 3F8h - 3FFh |
| COM2 | 2F8h - 2FFh |
| COM3 | 3E8h - 3EFh |
| COM4 | 2E8h - 2EFh |
| COM5 | 338h - 33Fh |
| COM6 | 238h - 23Fh |
| COM7 | 380h - 387h |
| COM8 | 280h - 287h |
| COM9 | 3A0h - 3A7h |

Table B2: "Standard" PC Serial Port Address

## B.2 INTERRUPT SELECTION - JUMPER AREA E2

The jumper area E2 selects interrupts for each UART channel. Eight different PC/104 IRQ lines can be selected, and each UART can be configured to drive any of the IRQ lines, with the restriction that each IRQ line can only be connected to one UART. Note that all four UART interrupts can be OR-ed together and the output of the OR gate can drive one IRQ line. This requires LK15 to be changed as described in section B.3.

Tables B3, B4, B5 and B6 list the E2 jumper settings for UART channels A, B, C and D respectively. If an interrupt is not required from a UART then do not fit any jumper. When all four interrupts are OR-ed together, Table B5 gives the jumper settings. In this case there must be only one jumper on E2.

| IRQ | Jumper E2 Setting for Channel... | | | |
|---|---|---|---|---|
| | A | B | C | D |
| IRQ9 (IRQ2) | A2 - A3 | B2 - B3 | A1 - A2 | B1 - B2 |
| IRQ3 | C2 - C3 | D2 - D3 | C1 - C2 | D1 - D2 |
| IRQ4 | E2 - E3 | F2 - F3 | E1 - E2 | F1 - F2 |
| IRQ5 | G2 - G3 * | H2 - H3 | G1 - G2 | H1 - H2 |
| IRQ10 | I2 - I3 | J2 - J3 * | I1 - I2 | J1 - J2 |
| IRQ11 | K2 - K3 | L2 - L3 | K1 - K2 * | L1 - L2 |
| IRQ14 | M2 - M3 | N2 - N3 | M1 - M2 | N1 - N2 |
| IRQ15 | O2 - O3 | P2 - P3 | O1 - O2 | P1 - P2 * |
| None | No Jumper | No Jumper | No Jumper | No Jumper |

Table B3: Interrupt Link Settings (* Default Setting)

### B.3 OR-ING INTERRUPTS

If interrupts are to be OR-ed, as decribed in section 2.2, then solder link area LK15 should be changed as shown below, and Table B5 above should be used to select the IRQ signal required.

| | |
|---|---|
| Interrupts OR-ed: | Set LK15 1-2 |
| Interrupts not OR-ed: | Set LK15 2-3 (default) |

### B.4 UART CLOCK SELECTION

The frequency of the UART clock can be selected at link area LK1. See section 3 for details.

| | |
|---|---|
| 1.843mhz: | Set LK1 3-4 (default) |
| 3.686mhz: | Set LK1 2-5 |
| 7.373mhz: | Set LK1 1-6 |

### B.5 RS-232 POWER-DOWN OPTIONS

The RS-232 transceivers can be powered down as described in section 4.1. The link settings are given below:

Controlled by SHDN pin:

| | |
|---|---|
| Channel A | link LK11 2-3 (default) |
| Channel B | link LK8 2-3 (default) |
| Channel C | link LK6 2-3 (default) |
| Channel D | link LK3 2-3 (default) |

Controlled by DTR pin:

| | |
|---|---|
| Channel A | link LK11 1-2 |
| Channel B | link LK8 1-2 |
| Channel C | link LK6 1-2 |
| Channe D | link LK3 1-2 |

Always off (for RS-485):

| | |
|---|---|
| Channel A | no link at LK11 |
| Channel B | no link at LK8 |
| Channel C | no link at LK6 |
| Channel D | no link at LK3 |

**B.6 RS-485 RECEIVE DATA SELECTION**

Each channel has a link which is set depending on whether RS-485 operation is being used, and whether full-duplex or half duplex operation is being used. This link determines how the UART 'receive data' pin (RxD) being driven.

Half-Duplex, RxD Driven only when RTS inactive:

Channel A link LK13 1-2 (default)
Channel B link LK9 1-2 (default)
Channel C link LK5 1-2 (default)
Channel D link LK2 1-2 (default)

Half-Duplex, RxD driven always:

Channel A link LK13 2-3
Channel B link LK9 2-3
Channel C link LK5 2-3
Channel D link LK2 2-3

Full-Duplex, RxD driven by receive twisted pair:

Channel A no link at LK13
Channel B no link at LK9
Channel C no link at LK5
Channel D no link at LK2

**B.7 RS-485 TRANSCEIVERS**

For RS-485 operation either one or two RS-485 transceiver chips need to be fitted for each UART channel. In addition the settings of two solder links per channel need to be considered.

For half-duplex operation:

For Channel A fit IC17
For Channel B fit IC12
For Channel C fit IC7
For Channel D fit IC3

For full-duplex operation:

For Channel A fit IC17 and IC18
For Channel B fit IC12 and IC13
For Channel C fit IC7 and IC8
For Channel D fit IC3 and IC4

The RS-232 transceivers need to be disabled, as indicated in section B.5 above. The source of the RxD needs to be set as indicated in section B.6 above.

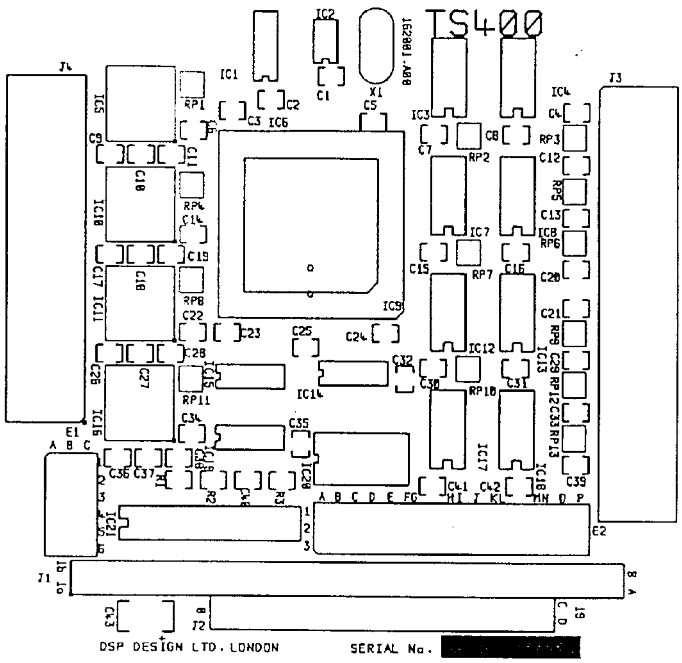
**B.8 FACTORY FITTED LINKS**

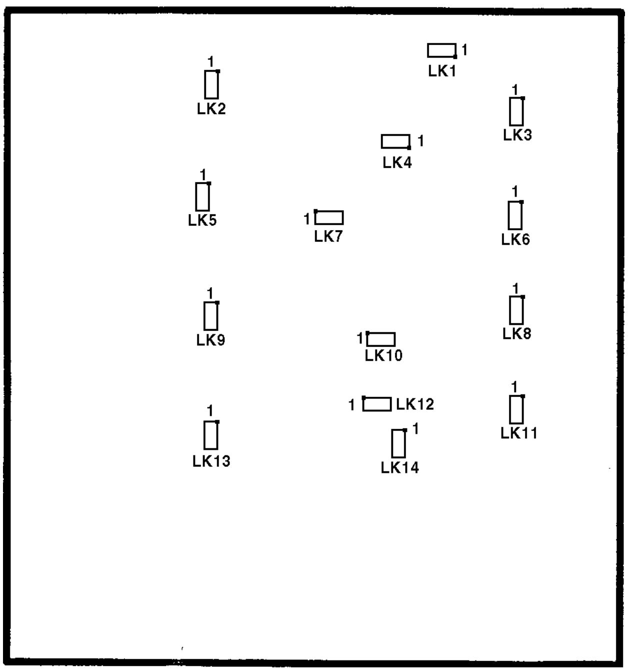
The following link settings are made at the factory and must not be changed:

LK4 no links fitted
LK7 no links fitted
LK12 link 1-2
LK14 no link fitted

## APPENDIX C - COMPONENT PLACEMENT DIAGRAM

This Appendix includes a component placement diagram for the TS400.





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## APPENDIX E - ORDERING INFORMATION

The DSP Design part numbers for the TS400 and related products are detailed below.

| | |
|---|---|
| TS400 | A four channel asynchronous serial port card for the PC/104 bus. |
| TS400-485KIT | TS400 RS485 upgrade kit. Contains two RS485 chips. |
| TRM-TS400 | TS400 Technical Reference Manual (This manual). |
| COMM-DRVDOS | Powerfull serial communications driver package. |

DSP Design manufacture a range of PC/104 processor boards, I/O boards and development systems. Contact your supplier for the latest details.

## APPENDIX F - SPECIFICATION

| | |
|---|---|
| Product: | TS400 |
| Description: | PC/104 four channel serial communications board. |
| PC/104 interface: | I/O mapped, 8-bit data bus. I/O addresses can be configured with jumpers. |
| Interrupts: | IRQ3, IRQ4, IRQ5, IRQ9, IRQ10, IRQll, IRQ14 and IRQ15 and are jumper selectable. |
| Connectors: | PC/104 J1 (64-pin) and J2 (40-pin) stack-through connectors.<br>J3 50-way right angle pin header for RS-485 connections.<br>J4 40-way right angle pin header for RS-232 connections. |
| Dimensions: | 90mm x 96mm (PCB) (3.55" x 3.775") |
| Weight: | 70g approx. |
| Temperature: | 0 - 70 degrees C operating. |
| Humidity: | 10% - 90% non-condensing. |
| Power Supplies: | +5V/80mA typical (RS-232 transceivers active, not connected),<br>125mA typical (RS-232 transceivers active, looped back),<br>45mA (shutdown asserted). |

## APPENDIX G: FAULT REPORTING

DSP Design mlakes every effort to ship products and documentation which are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a “Product Fault Report" form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form to your supplier.

Prior to returning a faulty product, please check the following:

1 The board has been correctly configured for the intended application (see earlier appendix for board installation details).

2. The power supplies are providing correct voltage levels.

3. Cabling to the board is sound and connected correctly.

4. Other cards in the system are known to be correctly configured and functioning.

5. **PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

*Your help with this will enable us* to *sort out your problem more quickly. Thank you.*

## PRODUCT FAULT REPORT

| | |
|---|---|
| CUSTOMER INFORMATION | PRODUCT INFORMATION |
| COMPANY NAME: | PRODUCT/DOCUMENT: |
| INDIVIDUAL CONTACT: | SERIAL NO: |
| PHONE NO: | DATE OF RETURN: |

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

IN WHAT CONFIGURATION IS THE BOARD USUALLY USED? (WHAT OTHER BOARDS, WHAT SOFTWARE ETC)?

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT: REPAIRED BY:

CHARGES TO BE INVOICED: E

DATE OF RETURN: RETURNED BY: