

**TPO24  
PC/104 Opto-Isolated Digital  
Input & Output Board**

**18th April 1995**

All information in this manual is believed to be accurate and reliable. However, no responsibility is assumed by DSP Design Limited for its use. Since conditions of product use are outside our control, we make no warranties express or implied in relation thereto. We therefore cannot accept any liability in connection with any use of this information. Nothing herein is to be taken as a licence to operate under or a recommendation to infringe any patents.

Whilst every effort has been made to ensure that this document is correct, errors can occur. If you find any errors or omissions please let us know, so that we can put this right.

All information contained in this manual is proprietary to DSP Design Limited and cannot be reproduced without the consent of DSP Design Limited. The circuit design and printed circuit board design are copyright of DSP Design Limited 1994.

DSP Design Umited  
1 Apollo Studios  
Chariton Kings Road  
London NW5 2SB  
England

# TPO24 Technical Reference Manual

*Innovation in Electronics Supply*

---



**CONTENTS**

I INTRODUCTION .....	4
2 BUS INTERFACE .....	5
3 PARALLEL I/O CHIP .....	5
4 OPTO-ISOLATED OUTPUTS .....	6
5 OPTO-ISOLATED INPUTS .....	7
APPENDIX A: SPECIFICATION .....	8
APPENDIX B: PIN ASSIGNMENTS .....	9
APPENDIX C: TP024 CONFIGURATION .....	14
APPENDIX D: COMPONENT PLACEMENT DIAGRAM .....	15
APPENDIX E: ORDERING INFORMATION .....	16
APPENDIX F: FAULT REPORTING .....	17
TABLE 1: TP024 ADDRESS MAP .....	5
TABLE B1: TP024 PC BUS CONNECTOR (J1) PIN ASSIGNMENTS .....	10
TABLE B2: TP024 AT BUS CONNECTOR (J2) PIN ASSIGNMENTS .....	11
TABLE B3: INPUT CONNECTOR (J3) PIN ASSIGNMENTS .....	12
TABLE B4: OUTPUT CONNECTOR (J4) PIN ASSIGNMENT .....	13

## 1 INTRODUCTION

The TP024 provides 12 lines each of opto-isolated digital inputs and outputs for use with PC/104 bus based systems. The TP024 is intended to provide a level of opto-isolation in low voltage systems. It must not be used to provide isolation from hazardous voltages. If you require high voltage isolation or high current capabilities then we suggest you use Opto-22 modules with the TP406 board, also manufactured by DSP Design.

The parallel I/O functions are provided by a uPD71055 chip. This is equivalent to the Intel 8255 chip. Twelve of the pins of the uPD71055 are buffered and drive opto-isolated outputs, and twelve pins receive inputs from opto-isolated inputs.

The key features of the TP024 are listed below:

- **12 lines of opto-isolated outputs.**
- **60mA current source/sink capability on each output.**
- **12 lines of opto-isolated inputs.**
- **All input and output pins are isolated from each other.**
- **I/O mapped - address jumper selectable.**
- **Single +5V power supply. Very low power operation possible.**
- **Complies with PC/104 specification Revision 2.2.**

**2 BUS INTERFACE**

The TP024 is mapped into the I/O space of the PC/104 bus. It is an 8-bit interface, requiring only the signals on the J1 PC/104 connector. The J2 connector is present, to allow stacking of PC/104 modules.

The TP024 occupies 4 I/O addresses, which can be set on 4-bit boundaries in the I/O space.

Address lines A2-A9 are fed to the address decoder chip. Address lines A10-A15 are ignored. Thus the TP024 will be aliased, or repeated, every 1k bytes throughout the PC/104 I/O space.

Jumper area E1 allows the board address to be set. To set a base address first convert your desired address to a binary number, and then set jumpers in E1 to match each of the binary bits corresponding to address bits A2 - A9. Appendix B gives details on configuring the board.

Within the 4 I/O locations allocated to the TP024, individual addresses are allocated as follows:

Offset	uPD71055 Register
0	Port A Data
1	Port B Data
2	Port C Data
3	Command

Table 1: TPO24 Address Map

Programming the chip is described in section 3. Sample code is available on the TC486 utility disk (TCUTILS), available from your supplier.

The PC/104 RESETDRV signal is used to reset the uPD71055 parallel I/O chip.

**3 PARALLEL I/O CHIP**

The parallel I/O functions are provided by a uPD71055 chip. This is equivalent to the Intel 8255 chip. The I/O pins of the uPD71055 chip are connected to the opto-isolators.

The programming of the uPD71055 chip for the TP024 is quite simple, since each of the 24 I/O pins are fixed in their functions, either as an input bit or as an output bit. The chip therefore has to be initialised once following reset, and thereafter output ports can be written to and input ports read from.

Users who desire a fuller understanding of the uPD71055 chip can refer to extracts from the data sheet which are contained in the TP406 Technical Reference Manual.

The chip can be initialised by writing a single byte to the command register, to set the mode and direction of each of the three ports. Assuming a base address for the TP024 of 220H the initialising can be done as follows (code in 8086 assembler):

```

MOV DX, 223H      address of Control Register
MOV AL, 83H      value to configure ports
OUT DX,AL        write to the chip
  
```

Once initialised, inputs can be read from uPD71055 Port B bits 0-7 and from Port C bits 0-3. Outputs can be set by writing to uPD71055 Port A bits 0-7 and Port C bits 4-7.

To read the state of an opto-isolated input, simply read the appropriate port and examine the desired bit. As an example, to examine the state of bit 3 of Port B do this:

MOV DX, 221 H	address of data port B
IN AL, DX	read the port
TEST AL, 3	examine bit 3

To write to an opto-isolated output, simply write to the appropriate port with the required data. Note that you cannot write to an individual bit - you must write to 8 bits (port A) or four bits (port C) at a time. However, it is possible to establish the current state of any output bits by reading from the port. Thus, to set bit 3 of output port A you could do the following:

MOV DX, 220H	address of data port A
IN AL, DX	read current value
OR AL, 8	set bit 3
OUT DX,AL	write it back again.

## 4 OPTO-ISOLATED OUTPUTS

There are twelve opto-isolated outputs. Each can provide a level of isolation in low voltage systems. The TP024 must not be used to provide isolation from hazardous voltages.

Each output is driven by one bit of the uPD71055 chip. Port A bits 0-7 provide 8 bits, and Port C bits 4-7 provide the other 4 bits.

Each uPD71055 bit is configured such that it must be driven to logic 1 in order for the photo-transistors across the opto-isolated barrier to turn on. As an example, if Port A bit 0 is set to logic 1 then current will be able flow between the the PPAO and PAO pins on connector J4. When the uPD71055 pin is set to logic 0 (or when the pin is an input) current will not flow.

Each opto-isolator includes a darlington photo-transistor in the output stage. The collector and emitter of this darlington transistor are brought out to separate pins on the connector J4 (in fact, each is brought out to two adjacent pins).

The collector must be at a higher (more positive) voltage than the emitter. The opto-isolator has a maximum current capability of 160mA, and can withstand up to 40V when it is off. When conducting the darlington transistor saturation voltage is about 700mV.

Care should be taken not to exceed the total power dissipation of the opto-isolator packages. Each package has four opto-isolators each with a maximum power rating of 200mW. The power dissipated by each opto-isolator is the current flowing through it multiplied by the saturation voltage (700mV) multiplied by the duty cycle. The sum of the power dissipations of the four opto-isolators must not exceed 800mW. DSP Design recommends that the power is kept well below this level, to improve reliability. If you require higher currents or higher open circuit voltages, or higher isolation voltages, then we suggest you use our TP406 board with Opto-22 modules.

There is a time constant associated with turning on and off the opto-isolators. The turn-on time is approximately 100us. The turn off time is dependent on the current through the opto-isolator. With a current of about 10mA the turn off time is about 1 mS. As the current increases the turn off time is reduced.

Section 2 above gives details of programming the uPD71055. Some sample code is available which demonstrates the programming of the opto-isolator board. This code is included in the TC486 Utilities Disk (TCUTILS).

## 5 OPTO-ISOLATED INPUTS

There are twelve opto-isolated inputs. Each can provide a level of isolation in low voltage systems. The TP024 must not be used to provide isolation from hazardous voltages.

Each input drives one bit of the uPD71055 chip. Port B bits 0-7 provide 8 bits, and Port C bits 0-3 provide the other 4 bits.

Each uPD71055 bit is configured such that current must flow through the opto-isolator input stage in order for the uPD71055 chip to detect a logic 1. As an example, if current flows from J3 pin PBBO to PBO then a logic 1 will appear at uPD71055 port B bit 0. When there is no voltage applied between pins PBBO and PBO, or when the pins are left unconnected, the uPD71055 will see a logic 0.

Each opto-isolator includes a photo-diode input stage. The anode and cathode of this diode are brought out to separate pins on the connector J3 (in fact, each is brought out to two adjacent pins).

The anode must be at a higher (more positive) voltage than the cathode. The photodiode has a voltage threshold of about 1V before appreciable current will flow.

The opto-isolator has a maximum input current capability of 80mA, and can withstand up to 6V when reverse biased. We recommend a forward current of 5-10mA, and protection of the photodiode with an external silicon diode if there is a chance of reverse polarity connections.

Single-in-line resistor networks (RP3, 5, and 8) are installed in sockets. Each 8-pin resistor network contains four resistors. These resistors are in series with the photo-diode, to limit the forward current and to allow a voltage to be applied at the J3 pins without external circuitry.

The resistors are 1k ohms. They are suitable for input voltages between about 5V and 10V. For voltages higher than about 10V the resistor should be changed to restrict the diode current to about 5mA.

Care should be taken not to exceed the total power dissipation of the resistor network packages. Each package has four resistors in it, and the package has a maximum power rating of 0.8W. The power dissipated by each resistor is (approximately) the input voltage squared, divided by the resistance multiplied by the duty cycle. The sum of the power dissipations of the four resistors must not exceed 0.8W. DSP Design recommends that the power is kept well below this level, to improve reliability.

There is a time constant associated with turning on and off the opto-isolators. The turn-on time is approximately 100us. The turn off time is about 100us.

Section 2 above gives details of programming the uPD71055. Some sample code is available which demonstrates the programming of the opto-isolator board. This code is included in the TC486 Utilities Disk (TCUTILS).

## APPENDIX A: SPECIFICATION

Product:	TP024
Description:	PC/104 Opto-isolated digital I/O board.
PC/104 interface:	I/O mapped (4 I/O addresses); 8-bit data bus.
Interrupts:	None.
Connectors:	PC/104 J1 (64-pin) and J2 (40-pin) stack-though connectors. Two 50-way right angle pin headers for opto-isolated inputs and outputs.
Outputs:	12 Opto-isolated outputs; 16mA max, 40V max.
Inputs:	12 opto-isolated inputs; 6V max reverse voltage.
Isolation:	Not for use with hazardous voltages! Recommended 40V maximum.
Dimensions:	90mm x 96mm (PCB) (3.55" x 3.775")
Weight:	60g approx.
Temperature:	0-70 degrees C operating. (Ask about industrial temperature range version).
Humidity:	10% - 90% non-condensing.
Power Supplies:	+5V 95mA typical (all opto-isolators off); 55mA typical (all output opto-isolators on).

## **APPENDIX B: PIN ASSIGNMENTS**

There are four connectors on the TP024. Connectors J1 and J2 are defined by the PC/104 specification, and are in effect the PC/AT bus signals. Connectors J3 and J4 are defined by DSP Design, and carry the I/O signals to and from the TP024. This Appendix gives the pin assignments of these connectors.

### **B.1 PC Bus Connector (J1)**

The PC bus connector (J1) is a 64-way stack-through connector which carries the PC/104 PC bus signals between the processor and the TP406. It carries all the signals required for 8-bit data transfers (the TP024 only performs 8-bit transfers).

The J1 connector has two parts - male and female - so that the TP024 can be stacked in a PC/104 board stack. The PC bus connector is used as the main set of signals between the TP024 and additional I/O boards, as well as being part of the mechanical system which secures the TP024 board to other PC/104 boards.

PC bus cards have 62 pins - rows a and b, and pins 1 to 31. The PC/104 boards have most of these signals present on the connector marked J1, as well as two extra pins. The two extra pins (32a and 32b) are two additional GND pins (the 0V power supply signal).

Table B1 lists the pin assignments of the PC bus connector, J1.

Pin	Signal	Pin	Signal
1a	/IOCHCHK	1b	0V (Gnd)
2a	SD7	2b	RESETDRV
3a	SD6	3b	+5V (VCC)
4a	SD5	4b	IRQ2/9
5a	SD4	5b	-5V *
6a	SD3	6b	DRQ2 *
7a	SD2	7b	-12V*
8a	SD1	8b	/ENDXFR *
9a	SD0	9b	+12V *
10a	IOCHRDY *	10b	(KEY)
11a	AEN	11b	/SMEMW *
12a	SA19 *	12b	/SMEMR *
13a	SA18 *	13b	/IOW
14a	SA17 *	14b	/IOR
15a	SA16 *	15b	/DACK3 *
16a	SA15 *	16b	DRQ3 *
17a	SA14 *	17b	/DACK1 *
18a	SA13 *	18b	DRQ1 *
19a	SA12 *	19b	/REFRESH *
20a	SA11 *	20b	CLK
21a	SA10 *	21b	IRQ7
22a	SA9	22b	IRQ6
23a	SA8	23b	IRQ5
24a	SA7	24b	IRQ4 *
25a	SA6	25b	IRQ3 *
26a	SA5	26b	/DACK2 *
27a	SA4	27b	TC *
28a	SA3	28b	BALE *
29a	SA2	29b	+5V (VCC)
30a	SA1	30b	OSC *
31a	SA0	31b	0V (Gnd)
32a	0V (Gnd)	32b	0V (Gnd)

Table B1: TPO24 PC Bus Connector (J1) Pin assignments

\* These signals are not used on TP406

**B.2 AT BUS EXTENSION CONNECTOR (J2)**

The J2 connector is defined by the PC/104 specification. It carries the signals required for 16-bit bus cycles, as used on AT expansion boards. None of the signals, except power supply signals, are used on the TP024.

The connector has two parts - male and female - so that the TP024 can be stacked in a PC/104 board stack. The AT bus connector is used to provide 16-bit data transfers (not used on the TP024) as well as being part of the mechanical system which secures the TP024 board to other PC/104 boards.

The pin assignments of J2 follow:

Pin	Signal	Pin	Signal
0c	0V (Gnd)	0d	0V (Gnd)
1c	/SBHE *	1d	/MEMCS16 *
2c	LA23 *	2d	/IOCS16 *
3c	LA22 *	3d	IRQ10 *
4c	LA21 *	4d	IRQ11 *
5c	LA20 *	5d	IRQ12 *
6c	LA19 *	6d	IRQ13 *
7c	LA18 *	7d	IRQ14 *
8c	LA17 *	8d	/DACK0 *
9c	/MEMR *	9d	DRQ0 *
10c	/MEMW *	10d	/DACK5 *
11c	SD8 *	11d	DRQ5 *
12c	SD9 *	12d	/DACK6 *
13c	SD10 *	13d	DRQ6 *
14c	SD11 *	14d	/DACK7 *
15c	SD12 *	15d	DRQ7 *
16c	SD13 *	16d	+5V (VCC)
17c	SD14 *	17d	/MASTER *
18c	SD15 *	18d	0V (Gnd)
19c	(KEY)	19d	0V (Gnd)

Table B2: TPO24 AT bUS Connector (J2) Pin Assignments

\* These signals are not used on the TP406

## B.3 50-way Opto-isolated Input Connector (J3)

J3 carries signals into the opto-isolators. The input connector, designated J3, is a 50-way connector situated along one of the edges of the TP024, perpendicular to J1 and J2.

The pin assignments for the 50-way J3 connector are given in Table B3. Pin 1 of the J3 connector is the pin nearest the angled corner of the J3 component outline marked on the PCB.

The Table B3 contains the signal name given to the input pins by DSP Design and the pin on the uPD71055 to which they connect. Note that each signal connects to two adjacent pins on the connector. The polarity is also indicated. The pin marked + needs to be at a higher potential than the pin marked minus

Pin	Signal	+/-	uPD71055 Pin	Pin	Signal	+/-	uPD71055 Pin
1	PPC0	+	Port C Bit 0	2	PPC0	+	Port C Bit 0
3	PC0	-	Port C Bit 0	4	PC0	-	Port C Bit 0
5	PPC1	+	Port C Bit 1	6	PPC1	+	Port C Bit 1
7	PC1	-	Port C Bit 1	8	PC1	-	Port C Bit 1
9	PPC2	+	Port C Bit 2	10	PPC2	+	Port C Bit 2
11	PC2	-	Port C Bit 2	12	PC2	-	Port C Bit 2
13	PPC3	+	Port C Bit 3	14	PPC3	+	Port C Bit 3
15	PC3	-	Port C Bit 3	16	PC3	-	Port C Bit 3
17	PPB0	+	Port B Bit 0	18	PPB0	+	Port C Bit 0
19	PB0	-	Port B Bit 0	20	PB0	-	Port C Bit 0
21	PPB1	+	Port B Bit 1	22	PPB1	+	Port C Bit 1
23	PB1	-	Port B Bit 1	24	PB1	-	Port C Bit 1
25	PPB2	+	Port B Bit 2	26	PPB2	+	Port C Bit 2
27	PB2	-	Port B Bit 2	28	PB2	-	Port C Bit 2
29	PPB3	+	Port B Bit 3	30	PPB3	+	Port C Bit 3
31	PB3	-	Port B Bit 3	32	PB3	-	Port C Bit 3
33	PPB4	+	Port B Bit 4	34	PPB4	+	Port C Bit 4
35	PB4	-	Port B Bit 4	36	PB4	-	Port C Bit 4
37	PPB5	+	Port B Bit 5	38	PPB5	+	Port C Bit 5
39	PB5	-	Port B Bit 5	40	PB5	-	Port C Bit 5
41	PPB6	+	Port B Bit 6	42	PPB6	+	Port C Bit 6
43	PB6	-	Port B Bit 6	44	PB6	-	Port C Bit 6
45	PPB7	+	Port B Bit 7	46	PPB7	+	Port C Bit 7
47	PB7	-	Port B Bit 7	48	PB7	-	Port C Bit 7
49	N/C			50	N/C		

Table B3: Input Connector (J3) Pin assignments

**B.4 50-way Opto-isolated Output Connector (J4)**

J4 carries signals out from the opto-isolators. The output connector, designated J4, is a 50-way connector situated along one of the edges of the TP024, perpendicular to J1 and J2.

The pin assignments for the 50-way J3 connector are given in Table B4. Pin 1 of the J4 connector is the pin nearest the angled corner of the J4 component outline marked on the PCB.

The Table B4 contains the signal names given to the output pins by DSP Design and the pins on the uPD71055 to which they connect. Note that each signal connects to two adjacent pins on the connector. The polarity is also indicated. The pin marked + needs to be at a higher potential than the pin marked minus (-)

Pin	Signal	+/-	uPD71055 Pin	Pin	Signal	+/-	uPD71055 Pin
1	PPA0	+	Port A Bit 0	2	PPA0	+	Port A Bit 0
3	PA0	-	Port A Bit 0	4	PA0	-	Port A Bit 0
5	PPA1	+	Port A Bit 1	6	PPA1	+	Port A Bit 1
7	PA1	-	Port A Bit 1	8	PA1	-	Port A Bit 1
9	PPA2	+	Port A Bit 2	10	PPA2	+	Port A Bit 2
11	PA2	-	Port A Bit 2	12	PA2	-	Port A Bit 2
13	PPA3	+	Port A Bit 3	14	PPA3	+	Port A Bit 3
15	PA3	-	Port A Bit 3	16	PA3	-	Port A Bit 3
17	PPA0	+	Port A Bit 0	18	PPA4	+	Port A Bit 4
19	PA0	-	Port A Bit 0	20	PA4	-	Port A Bit 4
21	PPA1	+	Port A Bit 1	22	PPA5	+	Port A Bit 5
23	PA1	-	Port A Bit 1	24	PA5	-	Port A Bit 5
25	PPA2	+	Port A Bit 2	26	PPA6	+	Port A Bit 6
27	PA2	-	Port A Bit 2	28	PA6	-	Port A Bit 6
29	PPA3	+	Port A Bit 3	30	PPA7	+	Port A Bit 7
31	PA3	-	Port A Bit 3	32	PA7	-	Port A Bit 7
33	PPA4	+	Port C Bit 4	34	PPC4	+	Port C Bit 4
35	PA4	-	Port C Bit 4	36	PC4	-	Port C Bit 4
37	PPA5	+	Port C Bit 5	38	PPC5	+	Port C Bit 5
39	PA5	-	Port C Bit 5	40	PC5	-	Port C Bit 5
41	PPA6	+	Port C Bit 6	42	PPC6	+	Port C Bit 6
43	PA6	-	Port C Bit 6	44	PC6	-	Port C Bit 6
45	PPA7	+	Port C Bit 7	46	PPC7	+	Port C Bit 7
47	PA7	-	Port C Bit 7	48	PC7	-	Port C Bit 7
49	N/C			50	N/C		

Table B4: Input Connector (J4) Pin assignments

## APPENDIX C: TP024 CONFIGURATION

There is one jumper area on the TP024. The value of the resistor networks may need to be changed depending on the input voltage. This Appendix describes how to configure the TP024.

### JUMPER AREA E1 - BASE ADDRESS

This jumper area allows the base address of the TP024 to be set. The required base address is converted to binary form and its bits A2 - A9 are set at jumper area E1 as indicated below.

If address A2=0	set E1 B1 -C1.	If address A2=1	set E1 A1-B1.
If address A3=0	set E1 B2-C2.	If address A3=1	set E1 A2-B2.
If address A4=0	set E1 B3-C3.	If address A4=1	set E1 A3-B3.
If address A5=0	set E1 B4-C4.	If address A5=1	set E1 A4-B4.
If address A6=0	set E1 B5-C5.	If address A6=1	set E1 A5-B5.
If address A7=0	set E1 B6-C6.	If address A7=1	set E1 A6-B6.
If address A8=0	set E1 B7-C7.	If address A8=1	set E1 A7-B7.
If address A9=0	set E1 B8-C8.	If address A9=1	set E1 A8-B8.

As an example, the TP024 base address is to be set to 320H. This is converted to binary form and bits 0 and 1 are ignored. This gives a binary number 11001000 (corresponding to A9 - A2). Using the above table the jumpers are set as follows:

A8-B8, A7-B7, B6-C6, B5-C5, A4-B4, B3-C3, B2-C2, B1-C1

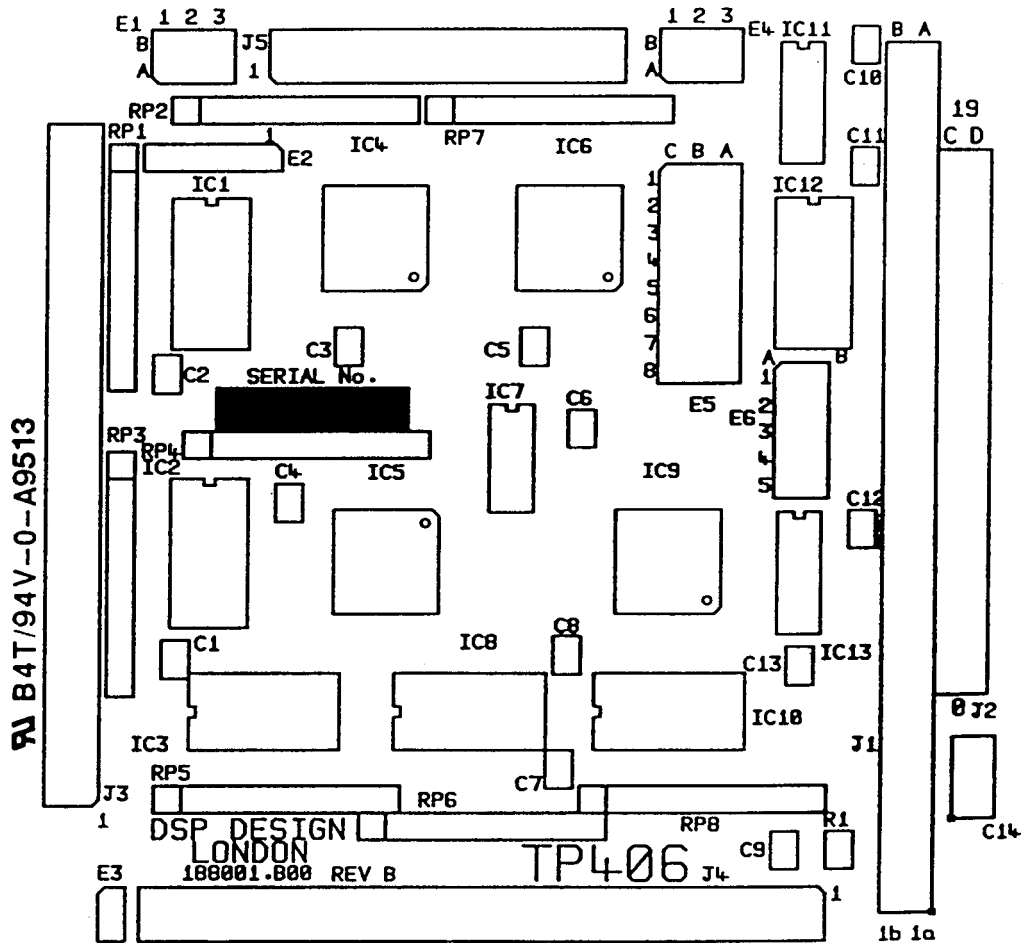
### RESISTOR NETWORKS - RP3, RP5 & RP8

In the default configuration the TP024 is optimised for input voltages in the 5V - 10V range. For voltages outside this range the resistor networks RP3, RP5 and RP8 may need to be changed to set the LED current to about 5mA. The resistor network is an 8-pin SIL package with four independent resistors. The optimum resistance can be calculated by;

$$\begin{aligned} R = V/I &= (V_{in} - V_{led})/5 \text{ Kohm} \\ &= (V_{in} - 1.1)/5 \text{ Kohm} \end{aligned}$$

**APPENDIX D: COMPONENT PLACEMENT DIAGRAM**

This appendix contains a component placement diagram for the TP024, which may be of help in locating components referred to in this manual.



## **APPENDIX E: ORDERING INFORMATION**

The DSP Design part number for the TP024 and related products are given below. For further information regarding other products from DSP Design please contact your supplier.

### **ORDER CODES**

TP024          PC/104 Opto-isolated I/O board

### **ACCESSORIES**

The following part numbers should be used to order various accessories for the TP024.

TCUTILS      TC486 utilities disk - includes sample software

DSP Design manufacture a range of PC/104 processor boards, I/O boards and development systems. Contact your supplier for the latest details.

**APPENDIX F: FAULT REPORTING**

DSP Design makes every effort to ship products and documentation which are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a "Product Fault Report" form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form to your supplier.

Prior to returning a faulty product, please check the following:

- 1 The board has been correctly configured for the intended application (see earlier appendix for board installation details).
2. The power supplies are providing correct voltage levels.
3. Cabling to the board is sound and connected correctly.
4. Other cards in the system are known to be correctly configured and functioning.
5. **PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

*Your help with this will enable us to sort out your problem more quickly. Thank you.*

## PRODUCT FAULT REPORT

CUSTOMER INFORMATION

COMPANY NAME:  
INDIVIDUAL CONTACT:  
PHONE NO:

PRODUCT INFORMATION

PRODUCT/DOCUMENT:  
SERIAL NO:  
DATE OF RETURN:

---

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

---

IN WHAT CONFIGURATION IS THE BOARD USUALLY USED? (WHAT OTHER BOARDS, WHAT SOFTWARE ETC)?

---

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT:

REPAIRED BY:

CHARGES TO BE INVOICED: E

DATE OF RETURN:

RETURNED BY: