

**TP406
PC/104 Digital I/O and Timer/Counter Board**

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TP406 Technical Reference Manual

Innovation in Electronics Supply



INTRODUCTION

The TP406 provides a range of parallel I/O and counter/timer functions for use with PC/104 bus based systems.

The parallel I/O functions are provided by two uPD71055 chips. These are equivalent to the Intel 8255 chip. The outputs of the uPD71055 chips are buffered by 74ACT245 chips, to give a high current source/sink capability.

The counter/timer functions are provided by two uPD71054 chips. These are equivalent to the Intel 8254 chip. The CLK, GATE and OUT pins are all made available to the user.

The key features of the TP406 are listed below:

- **40 lines of parallel I/O.**
- **24mA current source/sink capability.**
- **Pull-up resistors on most I/O pins.**
- **Option for connecting to Opto-22 style opto-isolated I/O modules.**
- **Six counter/timer channels with flexible connection options.**
- **I/O mapped - address jumper selectable.**
- **Option to interrupt processor.**
- **Single +5V power supply. Very low power operation possible.**
- **Complies with PC/104 specification Revision 2.2.**

BUS INTERFACE

The TP406 is mapped into the I/O space of the PC/104 bus. It is an 8-bit interface, requiring only the signals on the J1 PC/104 connector. The J2 connector is present, to allow stacking of PC/104 modules.

The TP406 occupies 16 I/O addresses, which can be set on 16-bit boundaries in the I/O space.

Address lines A4-A11 are fed to the address decoder chip. Address lines A12 and A13 must be set to 0. Address lines A14 and A15 are ignored.

Jumper area E5 allows the base address of the board to be set. To set a base address first convert your desired address to a binary number, and then set jumpers in E5 to match each of the binary bits corresponding to address bits A4 - A11. Appendix gives details on configuring the board.

Within the 16 I/O locations allocated to the TP406, individual addresses are allocated as follows:

| Offset | Chip | Register |
|--------|-------------|-----------------------|
| 0 | 71055 No. 1 | Port A Data |
| 1 | 71055 No. 1 | Port B Data |
| 2 | 71055 No. 1 | Port C Data |
| 3 | 71055 No. 1 | Command Register |
| 4 | 71055 No. 2 | Port A Data |
| 5 | 71055 No. 2 | Port B Data |
| 6 | 71055 No. 2 | Port C Data |
| 7 | 71055 No. 2 | Command Register |
| 8 | 71054 No. 1 | Counter 0 |
| 9 | 71054 No. 1 | Counter 1 |
| A | 71054 No. 1 | Counter 2 |
| B | 71054 No. 1 | Control Word Register |
| C | 71054 No. 2 | Counter 0 |
| D | 71054 No. 2 | Counter 1 |
| E | 71054 No. 2 | Counter 2 |
| F | 71054 No. 2 | Control Word Register |

Table 1: TP406 Address Map

See section 3 (Parallel I/O) and section 4 (Counter/Timers) for more information on how to program the uPD71055 and uPD71054 chips.

The TP406 can generate interrupts on the PC/104 bus. Interrupts can be generated by the counter/timers and in some limited circumstances by the parallel I/O chips. The PC/104 IRQ lines can be selected with jumper area E6. See Appendix C for information on configuring this jumper area. See sections on the parallel I/O and counter/timers for details of generating interrupts with the TP406.

The PC/104 RESETDRV signal is used to reset the parallel I/O and counter timer chips. The PC/104 CLK signal is optionally used as an input to the counter timer chips.

3 PARALLEL I/O

The parallel I/O functions are provided by two uPD71055 chips. These are equivalent to the Intel 8255 chip. The outputs of the uPD71055 chips are buffered by 74ACT245 chips, to give a high current source/sink capability.

Appendix E includes extracts from the 8255 data sheet. This can be used for instructions on programming the chips. In summary, the chips are initialised to the required mode by writing to Control Register. Thereafter data can be written to ports which have been configured as outputs, and can be read from ports which have been configured as inputs, by accessing the corresponding data register.

Some sample code is available which demonstrates the programming of the parallel I/O chips. UT This code is included in the TC486 Utilities Disk (Part number TCUTILS).

3.1 FACILITIES OF uPD71055 CHIPS

The uPD71055 chips are simple but versatile parallel interface chips. They each have three 8 bit ports, Port A, Port B and Port C.

Although the uPD71055 chips are able to operate in three different modes the details of the TP406 circuitry restricts operation to mode 0 only. This mode provides basic input/output operation. All three ports operate as programmable I/O ports.

3.2 INTERFACE OPTIONS

The TP406 is able to interact with external equipment through two interfaces. These are the general purpose I/O interface and the Opto-22 I/O Module Mounting Board interface.

Two 50 pin connectors take the buffered TP406 signals to external equipment. One of these connectors (J3) is used for the general purpose I/O interface and the other (J4) is used for the Opto-22 interface mode. The general purpose interface provides access to all 40 I/O signals. The Opto-22 interface provides 24 of the lines arranged to direct connection to the I/O module mounting boards manufactured by Opto-22.

Signals are buffered using standard "TTL level" signals. In fact the buffering is done with 74ACT245 CMOS drivers and receivers. The drivers can source or sink 24mA and the receivers respond to standard TTL threshold signals.

Details of the two interface options are given in sections 3.3 and 3.4 below.

3.3 GENERAL PURPOSE I/O

A 50-way connector (J3) and ribbon cable is used. Forty digital I/O lines are defined, and power supply signals are also included. The 40 I/O lines are divided into five groups of eight, referred to as Ports PA, PB, PC, PD and PE (these are not to be confused with Ports A, B and C of the uPD71055).

Some users may be familiar with the STEbus. Manufacturers of STEbus equipment have agreed on a common standard for I/O interfacing and a large number of products from a number of manufacturers support this standard. The J3 connector pin assignments comply with this standard.

3.3.1 PORTS PA, PB, PC, PD AND PE

On the TP406, uPD71055 No.1 (IC9) connects (via buffer chips) to three of the five ports on the connector, and uPD71055 No. 2 (IC5) connects to two. The remaining port on uPD71055 No.2 is used to control the direction and output enable pins of the I/O port buffer chips.

Table A3 in Appendix B summarises the relationship between the uPD71055 chips and the 50-way connector. Taking pin 23 as an example, this table shows that the connector signal PC1 (port C bit 1) is connected to uPD71055 No. 2 Port A bit 1.

It can therefore be seen that uPD71055 No.1 Ports A, B and C connect to I/O connector ports PA, PB and PE respectively, and that uPD71055 No. 2 Ports A and B connect to I/O connector ports PC and PD respectively.

This accounts for five of the six ports provided by the two uPD71055 chips. The final port, Port C on uPD71055 No.2, is used for controlling the I/O buffer chips. Specifically, four of the pins from this port control the direction of the buffers for ports PA, PB, PC and PD, and four of the pins drive the output enable lines on these ports. The allocation of these pins is summarised in Table 3.

Each of the five ports PA, PB, PC, PD and PE is buffered with a 74ACT245 chip. These are bidirectional transceiver chips, with a direction pin and an output enable pin. These control pins are driven by the uPD71055 No.2 Port C signals, so that the direction and activity of the ports can be individually controlled by software.

To configure Ports PA, PB, PC, and PD the appropriate bits must be set in uPD71055 No.2 Port C, as shown in Table 2. Note that the polarity of the direction bit is not the same for all ports. Port PE direction and enable control is discussed in section 3.3.2.

| uPD71055 No. 2 Port C Pin | Function |
|---------------------------|-------------------------------------|
| Bit 0 | PA Output Enable (1 to enable) |
| Bit 1 | PB & PE Output Enable (1 to enable) |
| Bit 2 | PC Output Enable (1 to enable) |
| Bit 3 | PD Output Enable (1 to enable) |
| Bit 4 | PA Direction (1 for output) |
| Bit 5 | PB & PE Direction (1 for output) |
| Bit 6 | PC Direction (0 for output) |
| Bit 7 | PD Direction (0 for output) |

Table 2: Control Function of uPD71055 No 2 Port C

3.3.2 PORT PE

A few words are necessary about port PE.

The enable pin of the port PE buffer is controlled by the same signal that controls port PB, as shown in Table 2.

The direction of port PE can be configured either as permanently output, permanently input or programmable. The direction is set at jumper area E2, as described in Appendix C. If the direction is controlled by software, then the direction of port PE is the same as that of port PB, as is shown in Table 2.

3.3.3 INITIALISATION

Users should take some care with initialising the uPD71055 ports, to ensure in particular that output ports do not drive external equipment with random data. Following a reset of the TP406, all ports on the uPD71055 chips are initialised as inputs, and all the ports on the I/O connector are disabled - that is presenting a high impedance. Users can thus rely on the TP406 being in a known state following reset and design their external circuitry accordingly.

To initialise the TP406 the following sequence is recommended.

Firstly initialise the uPD71055 chips. Mode 0 must be selected for all ports. Ports A, B and C in both chips should be set to inputs or outputs as required. Port C of uPD71055 No.2 must be set to be an output, since it controls the direction and output enable pins of the buffer chips. This initialisation is done by writing Mode Select Command words to the Control Registers of the uPD71055s.

Secondly, for all ports which are to be used as outputs, program the desired data byte to the appropriate uPD71055 Data Registers. This ensures that when the buffers are finally enabled the correct data will appear on the I/O connector pins.

Thirdly, program the Port C bits of the uPD71055 No.2 to select the direction of the buffers, and to enable them. When the buffers are enabled, those selected as inputs will pass the I/O connector data through to the uPD71055 input port pins, and those selected as outputs will drive the I/O connector pins with the data which has been set up on the uPD71055 output ports.

Table 3 summarises the values which should be written to the Control Registers to configure the three uPD71055 ports in each possible combination, assuming the uPD71055S are to be used in Mode 0 (simple I/O).

| Direction of | | | Command Word |
|--------------|--------|--------|--------------|
| Port A | Port B | Port C | |
| Out | Out | Out | 80H |
| Out | Out | In | 89H |
| Out | In | Out | 82H |
| Out | In | In | 8BH |
| In | Out | Out | 90H |
| In | Out | In | 99H |
| In | In | Out | 92H |
| In | In | In | 9BH |

Table 3: Selecting Port Directions

Users should avoid programming an uPD71055 port to be an output while its buffer chip is selected as an input. This would cause the uPD71055 and the buffer to drive against each other, and may damage one or both of the chips.

3.3.4 RESET STATE

On reset the uPD71055 ports will all be configured as inputs. Circuitry on the TP406 ensures that when the control port (port C of uPD71055 No.2) is set as an input, all of the buffer chips are disabled (port C set up as an input is equivalent to programming port C bits 0-3 as logic 0).

It can therefore be seen that the reset state of the TP406 is a 'safe' state, in that it leaves output devices in the off state. Pull-up resistors (10k ohms) on the output pins ensure that CMOS pins do not float.

3.3.5 ELECTRICAL CHARACTERISTICS

The driver chips used to buffer the uPD71055 signals are 74ACT245 devices.

These chips provide a 24mA output drive current (IOL), which should be sufficient for interfacing to most equipment over a short distance. If this is insufficient, versions of '245 chips are available with 48mA output current capability, but users should be realistic about the load they ask the TP406 to drive: 40 lines each sinking 48mA is 2A of current, which may cause noise or heating problems.

Pull-up resistors (10k ohms) on the output pins ensure that CMOS pins do not float.

3.4 OPTO-22 I/O MODULE MOUNTING BOARD INTERFACE

The second interface option provided by the TP406 is the ability to connect to I/O Module Mounting Boards. These mounting boards are available from an number of manufacturers, including Opto-22, Poffer and Brumfield, FR Electronics and International Rectifier. The boards provide sockets for a range of opto-isolated AC and DC input and output interface modules, and the boards share a defacto standard 50-way cable.

This 50-way cable provides connection for up to 24 I/O modules, as well as +5V and 0V connections. The I/O module mounting boards come in different sizes - boards are available for 4, 8, 16 and 24 I/O modules. They all use the same cable, but of course the small capacity boards utilise fewer of the data lines.

The Opto-22 I/O module interface uses three of the five uPD71055 ports which are used on the general purpose I/O interface. These are: uPD71055 No.1 Port A and uPD71055 No.2 Ports A and B. The same 74ACT245 buffer chips are used as are used for the general purpose I/O interface; the signals are routed in parallel to both connectors J3 and J4.

Table A4 in Appendix B lists the pin assignment of the I/O module mounting board cable, and specifies the uPD71055 pins which are associated with each of the signal lines. Connection to I/O module mounting cards is by the 50-way connector J4. As can be seen, all even numbered pins are 0V (GND) connections.

The I/O modules themselves require TTL level signals from the TP406. Output modules typically require a logic 0 to turn them on, and require the TP406 buffers to sink a current of around 10mA. Input modules provide a logic 0 to indicate an active input.

This is consistent with the operation of the TP406. On reset the TP406 ports which are connected to output modules will be disabled, so the output modules will be turned off. The output modules will remain switched off if the cable to the TP406 is not present, and will only be turned on when the TP406 ports are configured as outputs and driven to logic 0.

Section 3.3.3 and 3.3.4 give information about initialising the uPD71055s and about the reset state of the TP406 card. This information is also relevant for I/O module mounting board operation.

As can be seen from Table A4, 25 of the 50 pins on the J3 connector are 0V (GND) connections. Pin 49 can optionally provide +5V from the TP406 to operate the opto-isolation electronics of the I/O modules. If it is decided to supply +5V from the TP406, then a jumper (E3) must be installed. This is described in Appendix C. Note that most module mounting boards will have a link of their own which needs to be added if power is to be supplied from the cable.

The I/O module mounting boards all carry screw terminals which allow this +5V supply to be provided separately. Users are advised to check the specifications of the I/O modules they are using to determine the maximum current required from the +5V supply. If this is too large, considering the length of ribbon cable, then the external power source should be used.

4 COUNTER TIMER

The counter/timer functions are provided by two uPD71054 chips. These are equivalent to the Intel 8254 chip. The CLK, GATE and OUT pins are all made available to the user.

Appendix F includes extracts from the 8254 data sheet. This can be used for instructions on programming the chips. In summary, the chips are initialised to the required mode by writing to the Command Register. Thereafter counter/timer registers can be written to or read from. There is one register for each of the three counter/timers in each chip.

There are six identical counter/timers, named Channels 0 - 5. Each channel has three pins associated with it: a clock input (CLK), a gate input (GATE) and an output (OUT). All three pins are unconnected on the TP406 board, with the exception of 10k pull-up resistors on the CLK and GATE pins. Each pin is taken to the J5 connector for connection to external sources.

Jumper areas on the TP406 board allow, optionally, a buffered version of the PC/104 system clock to drive the clock inputs. The PC/104 clock (the CLK pin on J1) is usually driven at 8.33MHz by the TC386 and TC486 processors. On the TB8680 the CLK pin usually runs at 7.2MHz (or at a variable speed if Smart Sleep is enabled).

The counter/timers have a variety of programmable modes, such as free-running oscillators, event counters, one-shot timers etc. The data sheet in Appendix F gives full details on programming the timers.

Each timer is 16-bits in length, and counters could be cascaded through the J5 connector if required. Four of the six counter/timers can be used to generate interrupts - see Appendix C for details on configuring the TP406 to generate interrupts.

Some sample code is available which demonstrates the programming of the counter/timers. This code is included in the TC486 Utilities Disk (part number TCUTILS).

APPENDIX A: SPECIFICATION

| | |
|-------------------|---|
| Product: | TP406 |
| Description: | PC/104 digital I/O and counter/timer board. |
| PC/104 interface: | I/O mapped (16 I/O addresses);8-bit data bus. |
| Interrupts: | Timers can interrupt on IRQ2, IRQ5, IRQ6, IRQ7 |
| Connectors: | PC/104 J1 (64-pin) and J2 (40-pin) stack-through connectors. 50-way right angle pin headers (digital I/O). 50-way right angle pin header (Opto22 interface). 26-way right angle pin-header (counter/timers). |
| Digital I/O: | 40 logic level signals configurable as inputs or outputs 8 bits at a time. Uses 74ACT245 chips for 24mA source/sink,-capability. 10k pull-up resistors on I/O pins (except timer OUT pins). |
| Counter/timers: | Six 16-bit counter timers implemented in two 8254 type chips. Six programmable modes, including counter, free running oscillator, one-shot etc. Three pins for each channel are available on connector (CLK, GATE and OUT). |
| Dimensions: | 90mm x 96mm (PCB) (3.55' x 3.775") |
| Weight: | 70g approx. |
| Temperature: | 0 - 70 degrees C operating. (Ask about industrial temperature range version). |
| Humidity: | 10% - 90% non-condensing. |
| Power Supplies: | +5V / 97mA typical (all digital I/O set to inputs). |

APPENDIX B: PIN ASSIGNMENTS

There are five connectors on the TP406. Connectors J1 and J2 are defined by the PC/104 specification, and are in effect the PC/AT bus signals. Connectors J3, J4 and J5 are defined by DSP Design, and carry the I/O signals to and from the on-board peripherals. This Appendix gives the pin assignments of these connectors.

B.1 PC Bus Connector (J1)

The PC bus connector (J1) is a 64-way stack-through connector which carries the PC/104 PC bus signals between the processor and the TP406. It carries all the signals required for 8-bit data transfers (the TP406 only performs 8-bit transfers).

The J1 connector has two parts - male and female - so that the TP406 can be stacked in a PC/104 board stack. The PC bus connector is used as the main set of signals between the TP406 and additional I/O boards, as well as being part of the mechanical system which secures the TP406 board to other PC/104 boards.

PC bus cards have 62 pins - rows a and b, and pins 1 to 31. The PC/104 boards have most of these signals present on the connector marked J1, as well as two extra pins. The two extra pins (32a and 32b) are two additional GND pins (the 0V power supply signal).

Table B1 lists the pin assignments of the PC bus connector, J1.

| Pin | Signal | Pin | Signal |
|-----|-----------|-----|------------|
| 1a | /IOCHCHK | 1b | 0V (Gnd) |
| 2a | SD7 | 2b | RESETDRV |
| 3a | SD6 | 3b | +5V (VCC) |
| 4a | SD5 | 4b | IRQ2/9 |
| 5a | SD4 | 5b | -5V * |
| 6a | SD3 | 6b | DRQ2 * |
| 7a | SD2 | 7b | -12V* |
| 8a | SD1 | 8b | /ENDXFR * |
| 9a | SD0 | 9b | +12V * |
| 10a | IOCHRDY * | 10b | (KEY) |
| 11a | AEN | 11b | /SMEMW * |
| 12a | SA19 * | 12b | /SMEMR * |
| 13a | SA18 * | 13b | /IOW |
| 14a | SA17 * | 14b | /IOR |
| 15a | SA16 * | 15b | /DACK3 * |
| 16a | SA15 * | 16b | DRQ3 * |
| 17a | SA14 * | 17b | /DACK1 * |
| 18a | SA13 | 18b | DRQ1 * |
| 19a | SA12 | 19b | /REFRESH * |
| 20a | SA11 | 20b | CLK |
| 21a | SA10 | 21b | IRQ7 |
| 22a | SA9 | 22b | IRQ6 |
| 23a | SA8 | 23b | IRQ5 |
| 24a | SA7 | 24b | IRQ4 * |
| 25a | SA6 | 25b | IRQ3 * |
| 26a | SA5 | 26b | /DACK2 * |
| 27a | SA4 | 27b | TC * |
| 28a | SA3 | 28b | BALE * |
| 29a | SA2 | 29b | +5V (VCC) |
| 30a | SA1 | 30b | OSC * |
| 31a | SA0 | 31b | 0V (Gnd) |
| 32a | 0V (Gnd) | 32b | 0V (Gnd) |

Table B1: TP406 PC Bus Connector (J1) Pin assignments

* These signals are not used on TP406

B.2 AT BUS EXTENSION CONNECTOR (J2)

The J2 connector is defined by the PC/104 specification. It carries the signals required for 16-bit bus cycles, as used on AT expansion boards. None of the signals, except power supply signals, are used on the TP406.

The connector has two parts - male and female - so that the TP406 can be stacked in a PC/104 board stack. The AT bus connector is used to provide 16-bit data transfers (not used on the TP406) as well as being part of the mechanical system which secures the TP406 board to other PC/104 boards.

The pin assignments of J2 follow:

| Pin | Signal | Pin | Signal |
|-----|----------|-----|------------|
| 0c | 0V (Gnd) | 0d | 0V (Gnd) |
| 1c | /SBHE * | 1d | /MEMCS16 * |
| 2c | LA23 * | 2d | /IOCS16 * |
| 3c | LA22 * | 3d | IRQ10 * |
| 4c | LA21 * | 4d | IRQ11 * |
| 5c | LA20 * | 5d | IRQ12 * |
| 6c | LA19 * | 6d | IRQ13 * |
| 7c | LA18 * | 7d | IRQ14 * |
| 8c | LA17 * | 8d | /DACK0 * |
| 9c | /MEMR * | 9d | DRQ0 * |
| 10c | /MEMW * | 10d | /DACK5 * |
| 11c | SD8 * | 11d | DRQ5 * |
| 12c | SD9 * | 12d | /DACK6 * |
| 13c | SD10 * | 13d | DRQ6 * |
| 14c | SD11 * | 14d | /DACK7 * |
| 15c | SD12 * | 15d | DRQ7 * |
| 16c | SD13 * | 16d | +5V (VCC) |
| 17c | SD14 * | 17d | /MASTER * |
| 18c | SD15 * | 18d | 0V (Gnd) |
| 19c | (KEY) | 19d | 0V (Gnd) |

Table B2: TP406 AT bUS Connector (J2) Pin Assignments

* These signals are not used on the TP406

B.3 50-way Parallel I/O Connector (J3)

J3 carries signals to and from the parallel I/O buffers. The I/O connector, designated J3, is a 50-way connector situated along one of the edges of the TP406, opposite J1 and J2.

The pin assignments of the 50-way J3 connector are given in Table B3. Pin 1 is marked on the PCB artwork.

The Table B3 contains the signal name given to the I/O pin by DSP Design (port PA - PE), as well as referencing the uPD71055 chip and port number. Note for historical reasons the pin assignments for our Port PE are not very logical! Sorry!

| Pin | Signal | uPD71055 | Pin | Signal | uPD71055 |
|-----|----------|----------------|-----|----------|----------------|
| 1 | 0V (Gnd) | | 2 | 0V (Gnd) | |
| 3 | PA0 | Port A/1 Bit 0 | 4 | PA1 | Port A/1 Bit 1 |
| 5 | PA2 | Port A/1 Bit 2 | 6 | PA3 | Port A/1 Bit 3 |
| 7 | PA4 | Port A/1 Bit 4 | 8 | PA5 | Port A/1 Bit 5 |
| 9 | PA6 | Port A/1 Bit 6 | 10 | PA7 | Port A/1 Bit 7 |
| 11 | 0V (Gnd) | | 12 | PE3 | Port C/1 Bit 0 |
| 13 | PB0 | Port B/1 Bit 0 | 14 | PB1 | Port B/1 Bit 1 |
| 15 | PB2 | Port B/1 Bit 2 | 16 | PB3 | Port B/1 Bit 3 |
| 17 | PB4 | Port B/1 Bit 4 | 18 | PB5 | Port B/1 Bit 5 |
| 19 | PB6 | Port B/1 Bit 6 | 20 | PB7 | Port B/1 Bit 7 |
| 21 | 0V (Gnd) | | 22 | PE2 | Port C/1 Bit 4 |
| 23 | PC0 | Port A/2 Bit 0 | 24 | PC1 | Port A/2 Bit 1 |
| 25 | PC2 | Port A/2 Bit 2 | 26 | PC3 | Port A/2 Bit 3 |
| 27 | PC4 | Port A/2 Bit 4 | 28 | PC5 | Port A/2 Bit 5 |
| 29 | PC6 | Port A/2 Bit 6 | 30 | PC7 | Port A/2 Bit 7 |
| 31 | 0V (Gnd) | | 32 | PE1 | Port C/1 Bit 1 |
| 33 | PD0 | Port B/2 Bit 0 | 34 | PD1 | Port B/2 Bit 1 |
| 35 | PD2 | Port B/2 Bit 2 | 36 | PD3 | Port B/2 Bit 3 |
| 37 | PD4 | Port B/2 Bit 4 | 38 | PD5 | Port B/2 Bit 5 |
| 39 | PD6 | Port B/2 Bit 6 | 40 | PD7 | Port B/2 Bit 7 |
| 41 | 0V (Gnd) | | 42 | PE0 | Port C/1 Bit 2 |
| 43 | PE4 | | 44 | PE7 | |
| 45 | PE5 | | 46 | P36 | |
| 47 | -12V | | 48 | +12V | |
| 49 | +5V | | 50 | +5V | |

Table B3: TP406 I/O Connector (J3) Pin Assignments

B.4 Opto-22 I/O Connector (J4)

J4 carries signals to and from the parallel I/O buffers. The signals on this connector are also present on the J3 connector. However, on this connector 24 of the signals have been arranged in a sequence for driving Opto-22 module mounting boards.

The Opto-22 connector, designated J4, is a 50-way connector situated along one of the edges of the TP406, perpendicular to the J1 and J2 connectors.

The pin assignments of the 50-way connector J4 are given in Table B4. Pin 1 is marked on the PCB artwork.

| Pin | Signal | uPD71055 | Pin | Signal |
|-----|--------------|----------------|-----|----------|
| 1 | Module 23 | Port A/1 Bit 0 | 2 | 0V (Gnd) |
| 3 | Module 22 | Port A/1 Bit 1 | 4 | 0V (Gnd) |
| 5 | Module 21 | Port A/1 Bit 2 | 6 | 0V (Gnd) |
| 7 | Module 20 | Port A/1 Bit 3 | 8 | 0V (Gnd) |
| 9 | Module 19 | Port A/1 Bit 4 | 10 | 0V (Gnd) |
| 11 | Module 18 | Port A/1 Bit 5 | 12 | 0V (Gnd) |
| 13 | Module 17 | Port A/1 Bit 6 | 14 | 0V (Gnd) |
| 15 | Module 16 | Port A/1 Bit 7 | 16 | 0V (Gnd) |
| 17 | Module 15 | Port A/2 Bit 0 | 18 | 0V (Gnd) |
| 19 | Module 14 | Port A/2 Bit 1 | 20 | 0V (Gnd) |
| 21 | Module 13 | Port A/2 Bit 2 | 22 | 0V (Gnd) |
| 23 | Module 12 | Port A/2 Bit 3 | 24 | 0V (Gnd) |
| 25 | Module 11 | Port A/2 Bit 4 | 26 | 0V (Gnd) |
| 27 | Module 10 | Port A/2 Bit 5 | 28 | 0V (Gnd) |
| 29 | Module 9 | Port A/2 Bit 6 | 30 | 0V (Gnd) |
| 31 | Module 8 | Port A/2 Bit 7 | 32 | 0V (Gnd) |
| 33 | Module 7 | Port B/2 Bit 0 | 34 | 0V (Gnd) |
| 35 | Module 6 | Port B/2 Bit 1 | 36 | 0V (Gnd) |
| 37 | Module 5 | Port B/2 Bit 2 | 38 | 0V (Gnd) |
| 39 | Module 4 | Port B/2 Bit 3 | 40 | 0V (Gnd) |
| 41 | Module 3 | Port B/2 Bit 4 | 42 | 0V (Gnd) |
| 43 | Module 2 | Port B/2 Bit 5 | 44 | 0V (Gnd) |
| 45 | Module 1 | Port B/2 Bit 6 | 46 | 0V (Gnd) |
| 47 | Module 0 | Port B/2 Bit 7 | 48 | 0V (Gnd) |
| 49 | +5V (option) | | 50 | 0V (Gnd) |

Table B4: TP406 Opto-22 I/O Connector (J4) Pin Assignments

B.5 Counter Timer Connector (J5)

J5 carries signals to and from the Counter/Timer chips. The counter/timer connector, designated J5, is a 26-way connector situated along one of the edges of the TP406, perpendicular to J1 and J2.

The pin assignments of the 26-way J5 connector are given in Table B5. Pin 1 is marked on the PCB artwork.

| J5 | | uPD71054 Device No | Chip/pin | J5 | | uPD71054 Device No | Chip/pin |
|-----|--------|-----------------------|-----------|-----|--------|-----------------------|-----------|
| Pin | Signal | | | Pin | Signal | | |
| 1 | Gnd | | | 2 | CLK0 | 1 | Channel 0 |
| 3 | Gate0 | 1 | Channel 0 | 4 | OUT0 | 1 | Channel 0 |
| 5 | Gnd | | | 6 | CLK1 | 1 | Channel 1 |
| 7 | Gate1 | 1 | Channel 1 | 8 | OUT1 | 1 | Channel 1 |
| 9 | Gnd | | | 10 | CLK2 | 1 | Channel 2 |
| 11 | Gate2 | 1 | Channel 2 | 12 | OUT2 | 1 | Channel 2 |
| 13 | Gnd | | | 14 | CLK3 | 2 | Channel 0 |
| 15 | Gate3 | 2 | Channel 0 | 16 | OUT3 | 2 | Channel 0 |
| 17 | Gnd | | | 18 | CLK4 | 2 | Channel 1 |
| 19 | Gate4 | 2 | Channel 1 | 20 | OUT4 | 2 | Channel 1 |
| 21 | Gnd | | | 22 | CLK5 | 2 | Channel 2 |
| 23 | Gate5 | 2 | Channel 2 | 24 | OUT5 | 2 | Channel 2 |
| 25 | BCLK | | | 26 | Vcc | | |

Table B5: TP406 Counter/Timer Connector (J5) Pin assignments

APPENDIX C: TP406 CONFIGURATION

There are 6 jumper areas on the TP406. This Appendix describes how to configure the TP406.

JUMPER AREA E1 - COUNTERTIMER No.1 CLOCK SOURCE

This jumper area allows a buffered version of the PC/104 clock signal (called BCLK) to drive the CLK inputs of the uPD71054 counter/timer chip No. 1.

| | |
|-------------------------------|--------------|
| To drive Channel 0 with BCLK: | Set E1 A1-B1 |
| To drive Channel 1 with BCLK: | Set E1 A2-B2 |
| To drive Channel 2 with BCLK: | Set E1 A3-B3 |

JUMPER AREA E2 - PORT. E DIRECTION

This jumper area allows the direction of parallel I/O Port E to be set.

| | |
|--------------------------------------|---------------|
| Port E permanently an input: | Link pins 2-3 |
| Port E permanently an output: | Link pins 4-5 |
| Port E follows the port B direction: | Link pins 1-2 |

JUMPER AREA E3 - POWERING OPTO-22 MODULES

Jumper E3 allows the TP406 to provide +5V power to the Opto-22 I/O module mounting boards, via pin 49 of J4.

To provide +5V to the Opto-22 boards: Install E3.

JUMPER AREA E4 - COUNTER/TIMER No.2 CLOCK SOURCE

This jumper area allows a buffered version of the PC/104 clock signal (called BCLK) to drive the CLK inputs of the uPD71054 counter/timer chip No. 2.

| | |
|-------------------------------|---------------|
| To drive Channel 0 with BCLK: | Set E4 A1 -B1 |
| To drive Channel 1 with BCLK: | Set E4 A2-B2 |
| To drive Channel 2 with BCLK: | Set E4 A3-B3 |

JUMPER AREA E5 - BASE ADDRESS

This jumper area allows the base address of the TP406 to be set. The required base address is set to binary form and its A4 - A11 are set at jumper area E5 as indicated below:

| | | | |
|-------------------|---------------|--------------------|----------------|
| If address A4=0 | set E5 B1-C1. | If address A4=1 | set E5 A1 -B1. |
| If address A5=0 | set E5 B2-C2. | If address A5=1 | set E5 A2-B2. |
| If address A6=0 | set E5 B3-C3. | If address A6=1 | set E5 A3-B3. |
| If address A7=0 | set E5 B4-C4. | If address A7=1 | set E5 A4-B4. |
| If address A8=0 | set E5 B5-C5. | If address A8=1 | set E5 A5-B5. |
| If address A9=0 | set E5 B6-C6. | If address A9=1 | set E5 A6-B6. |
| If address A10=0 | set E5 B7-C7. | If address A10=1 | set E5 A7-B7. |
| If address A11 =0 | set E5 B8-C8. | If address A11 = 1 | set E5 A8-B8. |

As an example, the TP406 base address is to be set to 320H. This is converted to binary form and bits 0-3 are ignored. This gives a binary number 00110010 (corresponding to A11 - A4). Using the above table the jumpers are set as follows:

B8-C8, B7-C7, A6-B6, A5-B5, B4-C4, B3-C3, A2-B2, BI-CI

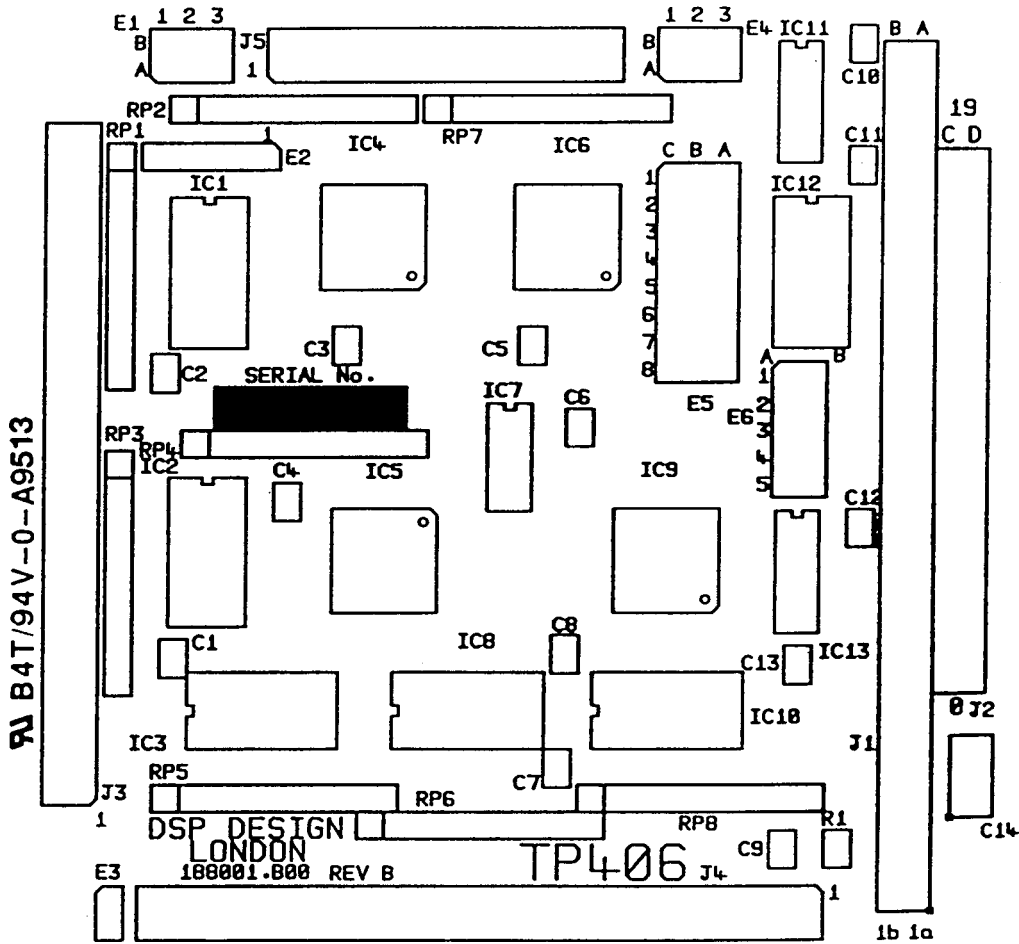
JUMPER AREA E6 - INTERRUPT ROUTING

This jumper area allows four of the counter/timer outputs and two parallel I/O lines to be jumpered to PC/104 interrupt pins. Not all options are available at once.

| | |
|---|----------------|
| For timer Channel 0 to interrupt on IRQ5: | Set E6 AI -A2. |
| For timer Channel 1 to interrupt on IRQ2: | Set E6 BI-B2. |
| For timer Channel 2 to interrupt on IRQ7: | Set E6 B4-B5. |
| For timer Channel 3 to interrupt on IRQ6: | Set E6 A4-A5. |
| For uPD71055 No. 1 port C bit 0 to interrupt on IRQ5: | Set E6 A2-A3. |
| For uPD71055 No. 1 port C bit 0 to interrupt on IRQ6: | Set E6 A3-A4. |
| For uPD71055 No. 1 port C bit 3 to interrupt on IRQ2: | Set E6 B2-B3. |
| For uPD71055 No. 1 port C bit 3 to interrupt on IRQ7: | Set E6 B3-B4. |

APPENDIX D: COMPONENT PLACEMENT DIAGRAM

The component placement diagram which follows may be of help in locating connectors and jumper areas which are referred to in this manual.



APPENDIX G: OPTION AND ORDERING INFORMATION

The DSP DESIGN part numbers for the TP406 and related products are given below. For further information regarding other products from DSP Design please contact your supplier.

| ORDERING CODES | DESCRIPTION |
|----------------|---|
| TP406 | PC/104 Parallel I/O and Counter/Timer Board |

| ACCESSORIES | DESCRIPTION |
|-------------|-------------|
|-------------|-------------|

The following part number(s) should be used to order various accessories:

| | |
|---------|--|
| TCUTILS | TC486 Utilities Disk (includes sample software). |
|---------|--|

DSP Design manufacture a range of PC/104 processor boards, I/O boards and development systems. Contact your supplier for latest details.

APPENDIX H: FAULT REPORTING

DSP Design makes every effort to ship products and documentation which are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a "Product Fault Report" form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form to your supplier.

Prior to returning a faulty product, please check the following:

- 1 The board has been correctly configured for the intended application (see earlier appendix for board installation details).
2. The power supplies are providing correct voltage levels.
3. Cabling to the board is sound and connected correctly.
4. Other cards in the system are known to be correctly configured and functioning.
5. **PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

Your help with this will enable us to sort out your problem more quickly. Thank you.

PRODUCT FAULT REPORT

CUSTOMER INFORMATION

COMPANY NAME:

INDIVIDUAL CONTACT:

PHONE NO:

PRODUCT INFORMATION

PRODUCT/DOCUMENT:

SERIAL NO:

DATE OF RETURN:

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

IN WHAT CONFIGURATION IS THE BOARD USUALLY USED? (WHAT OTHER BOARDS, WHAT SOFTWARE ETC)?

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT:

REPAIRED BY:

CHARGES TO BE INVOICED: E

DATE OF RETURN:

RETURNED BY: