# TC586

# PC/104 Target Board

# PC Compatible computers

# V1.3

# 20th August 1997



Whilst every effort has been made to ensure that this document is correct, errors can occur. If you find any errors or omissions please let us know, so that we can put this right.



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# 1 INTRODUCTION

## 1.1 OVERVIEW

To maintain our lead in advanced and highly integrated PC compatible computers, DSP Design have released a powerful Pentium-class processor board compliant with the PC/104 V2.3 specification.

This processor card offers a range of performance options since the TC586 can accept almost any processor with an 80486DX footprint. This includes the 486SX, 486DX, 486DX2, 486DX4 and 5x86 processors, from Intel, AMD, Cyrix and other manufacturers.

The board supports up to 32M bytes of DRAM . It also features the standard PC compatible serial ports, parallel port, keyboard interface, PS/2 mouse port and speaker controllers.

The TC586 is a single board PC/104 compatible computer that can operate as a stand-alone module or can be used in a system consisting of a number of other PC/104 modules.

Every TC586 is provided with Flash File System software, which converts the on-board 1M byte flash chip into a solid-state read/write disk drive.

A range of other PC/104 boards are available from DSP Design. The TC386 and TC486 are lower performance boards, but with the same connectors for interchangeability. The TX486 is similar to the TC586 and provides additional floppy and IDE disk interfaces. A wide range of I/O boards are available. Contact DSP Design for up-to-date information on other products in our range.

Note that there are two versions of the TC586 in the field. The REV C board incorporates a number of small enhancements. This manual covers both versions of the TC586, and where the two boards differ the differences are noted.

## 1.2 TC586 FEATURES

- **Choice of processors: 486SX, 486DX, 486DX2, 486DX4 or 5x86, running with a motherboard clock rate of 25MHz, 33MHz or 40MHz. (The DX2, DX4 and 5x86 processors internally multiply the motherboard clock rate to achieve internal clock rates of up to 133MHz).**
- **PC/104 V2.3 16-bit bus interface for wide compatibility.**
- **COM1 and COM2 RS-232 serial ports - COM2 is user-configurable as RS-485.**
- **The COM2 serial port can be optionally configured for IRDA-compatible infrared serial communications.**
- **Bi-directional Centronics parallel port. EPP and ECP compatible.**
- **Up to 32M bytes of DRAM. DRAM is implemented with a user-installable 72-pin SO DIMM module (small outline, dual-in line memory module).**
- **1M byte flash memory for BIOS and solid state disk. A Flash File System is provided with every TC586, to provide a read-write logical disk drive. A 2M byte chip can be fitted, subject to a minimum order quantity.**
- **Keyboard, PS/2 mouse and sound ports.**
- **Powered by a single 5V supply. A switched mode power supply is provided to efficiently produce 3.3V or 3.45V for processors which require these voltages.**
- **AT compatible calendar/clock chip uses external battery.**
- **A 512 byte size serial EEPROM is provided to retain set-up parameters in the absence of an external battery. Space is available for user data also.**
- **Reset, power supply monitor and watchdog timer circuitry.**
- **Expansion is by way of a full-function PC/104 bus which complies with the V2.3 version of the PC/104 bus specification.**

- **The TCDEV Development System provides all the facilities to get your TC586 running quickly, and is recommended for fast product development.**
- **Pin compatible with the TC386, TC486 and TX486 processors.**

### 1.3 PC/AT COMPATIBILITY

The TC586 offers an extremely high degree of compatibility with the IBM PC family of computers. This compatibility extends from the MS-DOS level, through BIOS-level compatibility to register-level compatibility.

The processor used on the TC586 board is supported by the FTD4591 motherboard chip. The FTD4591 includes on-chip peripherals - timers, interrupt controller, DMA controller etc. These are software compatible with equivalent Intel peripheral chips used on the original IBM PC and PC/AT.

In addition to the I/O resources in the FTD4591, the chip provides other features. A calendar/clock circuit and speaker port are included, and the chip looks after clock generation, address decoding, expansion bus timing, memory mapping and various other functions.

Around the FTD4591 chip DSP Design has integrated a keyboard and mouse controller, two serial ports and a Centronics parallel port. These peripherals are software and hardware compatible with the IBM PC/AT.

### 1.4 PC/104 AS A PC EXPANSION BUS

Users can operate the TC586 as a single board computer. If expansion is required I/O boards can be accessed via the PC/104 interface provided on the TC586.

The PC/104 bus is a compact version of the IEEE P996 (PC and PC/AT) bus, optimized for embedded systems applications. DSP Design and other PC/104 manufacturers offer a wide range of I/O boards that will work with the TC586, in the same manner that a conventional PC can be enhanced by the addition of expansion boards.

The PC/104 I/O card range includes analogue and digital I/O cards, serial comms, local area network boards and other specialist functions. DSP Design manufactures a number of PC/104 modules and we are committed to expanding this range.

It is the policy of DSP Design to introduce, where appropriate, new PC/104 I/O cards which are software compatible with similar cards for the IBM PC. This has the tremendous advantage of allowing users to make use of the software that has already been written for the IBM PC cards.

### 1.5 THE TC586 ARCHITECTURE

The block diagram in Figure 1 shows the architecture of the TC586. The processor accesses local DRAM and Flash memory. The FTD4591 chip performs a range of housekeeping and glue logic functions, as well as providing timer, interrupt, DMA, speaker and memory mapping facilities. The Super I/O chip includes serial and parallel I/O functions as well as the keyboard and mouse controller. This chip is connected to the internal buses.

Finally a 16-bit PC/104 interface allows the TC586 to perform memory and I/O accesses to the PC/104 bus. The FTD4591 interrupt and DMA controllers are used by the on-board peripherals as well as being connected to the expansion bus.

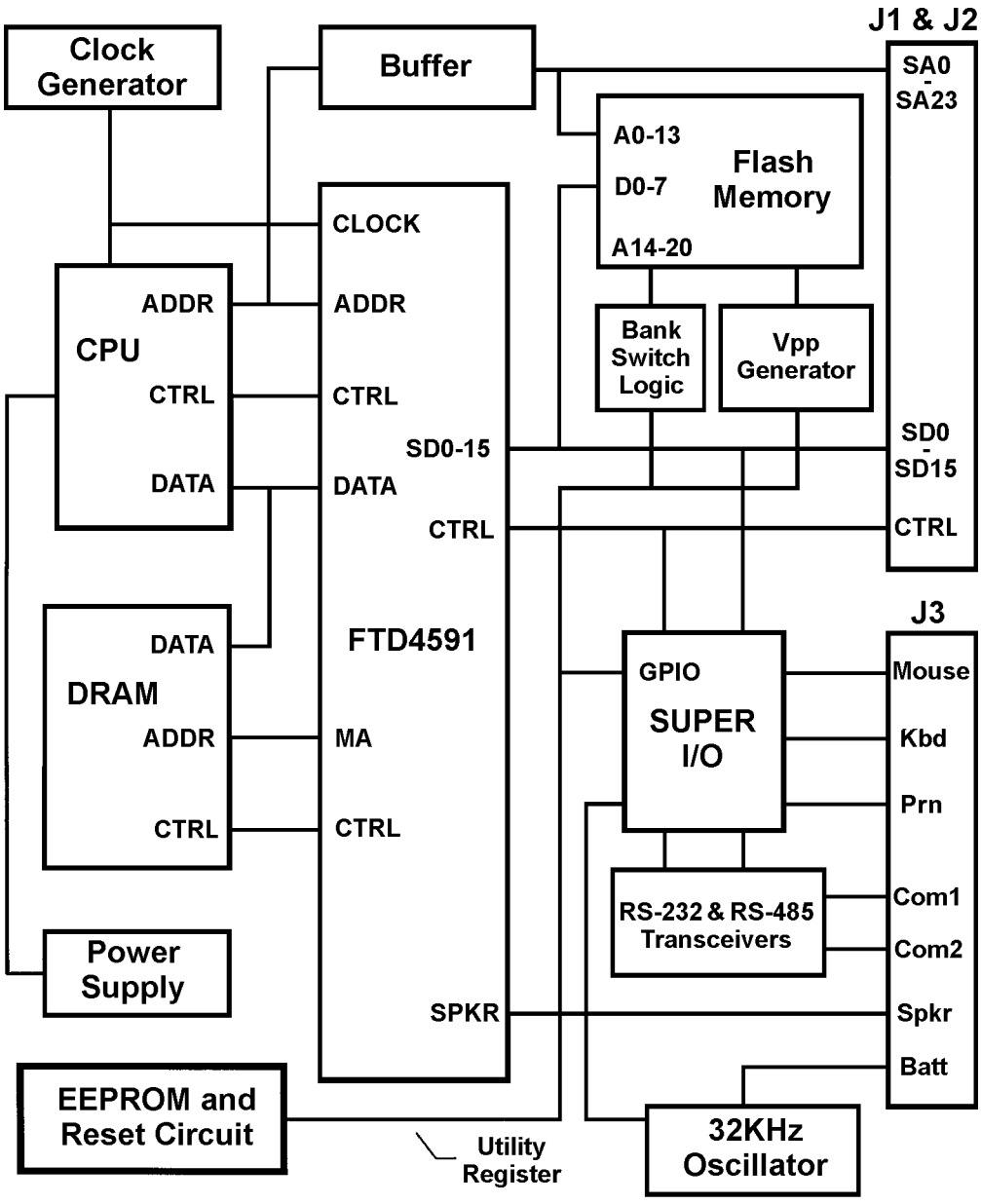



Figure 1: TC586 Block Diagram

### 1.6 GETTING STARTED QUICKLY

This manual gives all of the information that most users will need in order to operate the TC586. This section gives a quick introduction to getting started. More details on configuring the board are given in Appendix B: TC586 Setup Procedure. Those people who have special requirements may require further information. If this is the case our support engineers will be pleased to help you, but please read the manual first.

DSP Design strongly recommend developing with the TCDEV Development System, as in our experience this significantly reduces development time and users' technical problems.

The TCDEV is a PC/104 based development platform. Its features include an on board VGA graphics controller with 15 pin VGA connector, a floppy and hard disk controller, a floppy drive plus cable, a small prototyping area, a full PC/AT slot for interfacing standard PC and PC/AT bus cards to the PC/104 bus and a battery for CMOS RAM backup.

The TCDEV has all the standard PC connectors for interfacing to the outside world. These include two serial port 9 way D-type connectors, a parallel port 25 way D-type connector, a 5 pin DIN keyboard connector and a PS/2 style mouse connector.

DSP Design also supply the TCPSU which is a compact 3OW power supply with cabling to make it easy to use with the TCDEV.

Most users will find getting started with the TC586 and TCDEV simplicity itself. The TC586 plugs directly onto the TCDEV and a 50-way ribbon cable connects the TC586 J3 I/O socket to the TCDEV I/O socket. This links the serial, parallel and keyboard etc onto the TCDEV and in turn to the PC compatible connectors mounted on the edge of the TCDEV board.

There are two styles of TCDEV in the field. The revision B TCDEV boards can be identified by having only one site for PC/104 boards, and only one power LED. The revision C and later TCDEV boards have two sites for PC/104 boards, and eight diagnostic LEDs in a row as well as the power LED. The next two sections describe TC586 operation with each of the TCDEV variants.

#### 1.6.1 USING REV B TCDEV DEVELOPMENT SYSTEM

To use the system first install a DRAM DIMM module in the TC586 DRAM socket, observing its polarity, and observing proper anti-static precautions. The DIMM socket has a lug which engages with a cut-out on the module, which prevents incorrect installation.

If not already installed, plug the processor chip into the TC586 processor chip socket. Refer to APPENDIX B for details of how to install the processor chip correctly.

Various links may need to be set according to the type of processor chip installed. Refer to APPENDIX B for details on link configuration. Do not power-on the TCDEV TC586 with incorrect link settings as damage may result.

Enable the disk controllers and VGA graphics on the TCDEV. This is done by setting the three jumpers at jumper areas E3, E4 and E5 to the "EN" position. Ensure there are jumpers between positions 1 & 12, and 4 & 9 at jumper area El. The battery backup jumper should be set between positions 1 & 2 at jumper area E2. Remove the VGA BIOS EPROM from its socket on the TCDEV.

Plug the TC586 onto the TCDEV and connect the J3 I/O connector between the two boards. **Failure to connect the 50-way cable correctly may damage the equipment.**

Connect but do not switch on the TCPSU. (Note that the TCPSU power connector is polarized. Ensure that the locking tab on the power supply cable mates with the locking tab on the TCDEV connector). Connect the power supply earth wire to an earth spade terminal on the TCDEV. **Failure to connect the power supply cable assembly correctly may damage the equipment.**

Connect the keyboard and VGA monitor to the appropriate connectors.

Insert a bootable MS-DOS system disk into the TCDEV floppy disk drive and switch the power supply on. The computer should begin booting. Press the DEL key before or during the memory test to enter the Setup program. Select AUTO CONFIGURATION WITH OPTIMAL SETTINGS to load the optimal BIOS settings into CMOS. Select the SAVE SETTINGS AND EXIT option to reboot the TC586 with the new settings.

You should now boot DOS from the floppy disk drive on the TCDEV.

An alternative to using floppy disks is to make use of the hard disk controller already fitted to the TCDEV. Install a hard disk drive on the TCDEV IDE connector, re-enter the Setup program, and select the AUTODETECT HARD DISK option. Save the settings and exit. Section 3.7 has more details on the IDE interface. A Flash File system is also provided with the TC586. Section 6.4 has details of the Flash File System.

When development is complete the TC586 is removed from the TCDEV Development System. It can then operate stand-alone, or used with other PC/104 modules such as the TV750 VGA graphics module. Please contact your supplier for more information.

Note that as standard the TC586 processor includes a VGA BIOS for the 65535 VGA graphics controller chip on REV D and later TCDEV development systems. This BIOS will also work with the VG-660 VGA controller installed on the REV B TCDEV. The correct VG-660 VGA BIOS is provided on the TC586 utility disk, should you want to change it. You will find that when the TC586 is removed from the TCDEV the VGA BIOS will beep several times, indicating that it cannot find a VGA controller chip. You may wish to reprogram the flash memory with a BIOS image which does not contain a VGA BIOS to remedy this.

### 1.6.2 USING REV D OR LATER TCDEV DEVELOPMENT SYSTEM

To use your system install your DRAM DIMM module in the TC586 DRAM socket, observing its polarity, and observing proper anti-static precautions. The DIMM socket has a lug which engages with a cut-out on the module, which prevents incorrect installation.

If not already installed, plug the processor chip into the TC586 processor chip socket. Refer to APPENDIX B for details of how to install the processor chip correctly.

Various links may need to be set according to the type of processor chip installed. Refer to APPENDIX B for details on link configuration. Do not power-on the TCDEV TC586 with incorrect link settings as damage may result.

Enable the disk controllers and VGA graphics on the TCDEV. This is done by setting the three jumpers at jumper areas E3, E4 and E5 to the “EN” position. Ensure there are jumpers between positions 1 & 12, and 4 & 9 at jumper area El. The battery backup jumper should be set between positions 1 & 2 at E2. The status LED jumpers at E7 should both be set in the 1 - 2 position. At jumper area E6 set all jumpers to the DIS position.

Plug the TC586 onto the TCDEV and connect the J3 I/O connector between the two boards. It is probably best to use the J15 and J16 PC/104 connectors, and mount the TC586 face up, but you can also use the Jl and J2 connectors, and mount the TC586 face down. In either case ensure that pin 1 of the TCDEV 50-way connector J3 goes to pin 1 of the TC586. **Failure to connect the 50-way cable correctly may damage the equipment.**

Connect but do not switch on the TCPSU. (Note that the TCPSU power connector is polarized. Ensure that the locking tab on the power supply cable mates with the locking tab on the TCDEV connector). Connect the power supply earth wire to an earth spade terminal. On REV D TCDEVs this terminal is soldered to the printer connector. **Failure to connect the power supply cable assembly correctly may damage the equipment.**

Connect the keyboard and VGA monitor to the appropriate connectors.

Insert a bootable MS-DOS system disk into the TCDEV floppy disk drive and switch the power supply on. The computer should begin booting. Press the DEL key before or during the memory test to enter the Setup program. Select AUTO CONFIGURATION WITH OPTIMAL SETTINGS to load the optimal BIOS settings into CMOS.

Select the SAVE SETTINGS AND EXIT option to reboot the TC586 with the new settings.

An alternative to using floppy disks is to make use of the hard disk controller already fitted to the TCDEV. Install a hard disk drive on the TCDEV IDE connector, re-enter the Setup program, and select the AUTODETECT HARD DISK option. Save the settings and exit. Section 3.7 has more details on the IDE interface. A Flash File system is also provided with the TC586. Section 6.4 has details of the Flash File System.

When development is complete the TC586 is removed from the TCDEV Development System. It can then operate stand-alone, or used with other PC/104 modules such as the TV750 VGA graphics module. Please contact your supplier for more information.

Note that as standard the TC586 processor includes a VGA BIOS for the 65535 VGA graphics controller chip on REV D and later TCDEV development systems. This BIOS will also work with the VG-660 VGA controller installed on the REV B TCDEV. You will find that when the TC586 is removed from the TCDEV the VGA BIOS will beep several times, indicating that it cannot find a VGA controller chip. You may wish to reprogram the flash memory with a BIOS image which does not contain a VGA BIOS to remedy this.

## 2 PROCESSOR, MEMORY AND FTD4591 CHIP

The TC586 single board computer contains one of a number of processor chips, each of which is PC compatible but which differ in their processing power. There is one DIMM DRAM socket. The standard TC586 is supplied without processor or memory, allowing you to choose the processor and memory to suit your application. Processor and DRAM options are detailed in Appendix D, Options and Ordering Information.

### 2.1 PROCESSOR

The TC586 can be fitted with a variety of processors which are pin compatible with the Intel 80486DX. Most processors from most manufacturers can be fitted, although DSP Design recommends the Texas Instruments 80486DX2-66 as an inexpensive option and the SGS Thompson 5x86 as a high-performance option.

The performance of the TC586 may be gauged by the processor performance ratings produced by the Norton SI and the Ziff-Davis Winstone 96 programs as shown in Table 1. This table also gives typical power consumption figures for the TC586.

| CPU Type | Mfgr | Local Bus Speed (MHz) | CPU Speed (MHz) | Norton Rating | Winstone 95 Rating | | TC586 Power (mA) |
|---|---|---|---|---|---|---|---|
| | | | | | 16-Bit | 32-Bit | |
| 80486DX-33 | Intel | 25 | 25 | 39.5 | 29.3 | 33.0 | 556 |
| | | 33 | 33 | 52.7 | 39.6 | 44.5 | 706 |
| 80486DX2-66 | | 25 | 50 | 79.0 | 39.3 | 40.9 | 935 |
| | | 33 | 66 | 105.3 | 53.5 | 55.5 | 1100 |
| | TI | 25 | 50 | 110.6 | 31.6 | 40.9 | 470 |
| | | 33 | 66 | 147.5 | 42.6 | 55.1 | 552 |
| 80486DX2-80 | | 40 | 80 | 177.1 | 51.5 | 66.8 | 662 |
| 80486DX4-100 | | 25 | 75 | 164.7 | 34.2 | 44.5 | 618 |
| | | 33 | 100 | 219.6 | 46.3 | 60.3 | 749 |
| ST486DX2-66 | SGS | 25 | 50 | 110.6 | 31.3 | 40.9 | 747 |
| | | 33 | 66 | 147.5 | 42.6 | 55.2 | 893 |
| ST486DX2-80 | | 40 | 80 | 187.0 | 51.6 | 66.6 | 1000 |
| ST486DX4-100 | | 25 | 75 | 164.7 | 34.3 | 44.6 | 653 |
| | | 33 | 100 | 219.6 | 46.5 | 60.6 | 959 |
| ST5x86-100 | | 25 | 75 | 152.7 | 49.3 | 48.3 | 755 |
| | | 33 | 100 | 203.7 | 66.4 | 65.5 | 967 |
| AM486DX4-100 | AMD | 25 | 75 | 117.8 | 39.8 | 37.7 | 609 |
| | | 33 | 100 | 157.2 | 58.2 | 58.7 | 778 |
| AM486DX4-120 | | 33 | 100 | 165.8 | 58.5 | 59.0 | 963 |
| | | 40 | 120 | 188.6 | 69.9 | 70.9 | 1150 |
| AM5x86-133 | | 25 | 100 | 156.1 | 50.2 | 49.3 | 790 |
| | | 33 | 133 | 208.2 | 67.8 | 66.9 | 1030 |

Table 1: TC586 Performance Ratings

The above measurements were made with a 2-chip 4M byte DIMM module installed (DIMM module part number THL321050ATG-6). Power consumption figures were on average 160mA more when using an eight-chip 16M byte DIMM module. We assume that the higher current is related to the number of DRAM chips used on the module, rather than the memory capacity per se.

Users should make their own decision concerning cooling of the processor. The processors will dissipate between 1.5W and 5W, depending on processor type, operating voltage and speed (see Table 1 for overall power consumption - all except about 170mA of the current goes to the processor), and may get quite hot. Most chip manufacturers recommend an heat sink and/or a fan to keep the temperature of the processor down. The cooler a chip is the more reliable it will be. A fan or fan and heatsink combination can be fitted to the processor, or a fan could be provided in the enclosure along with the PC/104 boards. Connector J4 can be used to provide power for a fan.

As an alternative, the enclosure could be designed so that part of the enclosure acted as the heat sink. Thermal materials are available to provide a good thermal bond between the CPU and the case.

DSP Design can provide a heatsink, and a combined heatsink/fan. These are attached with thermally conductive double-sided adhesive tape.

### 2.2 FTD4591 CHIP

The TC586 computer is centered around the FTD4591 chip. This is a complex ASIC which provides a number of timing, control, address decoding functions and which includes a number of PC/AT compatible I/O peripheral circuits.

These peripherals include two 8237 compatible DMA control units (8 channels), one 8254 compatible timer control unit (3 channels), two 8259 compatible interrupt control units (15 interrupts), MC146818 compatible calendar/clock and CMOS RAM chip.

The other functions provided by the FTD4591 are:

- Memory controller with on-board memory mapping registers
- PC/104 bus interface and conversion logic
- Peripheral I/O address decoding

The majority of the peripheral functions are the same on all IBM PC/AT compatible computers. This includes the timers, interrupt controllers and DMA controllers as well as registers such as the NMI and speaker inhibit registers, fast reset and A20 gate registers. Software which accesses the IBM PC/AT peripherals will have the same effect when running on the TC586, giving rise to a high degree of PC-compatibility.

The FTD4591 chip also includes a number of internal configuration registers. These registers are unique to the FTD4591 chip. They control timing on the expansion bus, shadow RAM, DRAM configuration, memory mapping and so forth. They are initialized by the BIOS and will not normally need to be accessed by the user.

### 2.3 DRAM

The main memory of the TC586 consists of Dynamic RAM (DRAM) chips. The chips are mounted on a small 72-pin printed circuit board called a DIMM modules (dual-in-line memory module). Four options are available:

- **4M bytes**
- **8M bytes**
- **16M bytes**
- **32M bytes**

The standard configuration of the TC586 is to have no DRAM fitted. DIMM modules must be ordered separately and fitted into the DIMM socket on the TC586. See Appendix D: TC586 Options and Ordering Information.

The use of DIMM modules DRAM memory means that the DRAM configuration can be altered at a later stage. DSP Design carry stock of the DIMM modules described above. Care must be taken when handling the TC586 and associated components. Ensure that all anti-static handling precautions are taken. See Appendix B: TC586 Setup Procedure for instructions on installing DIMM modules.

Registers within the FTD4591 chip allow DRAM timing to be optimised according to CPU speed and DRAM access time. At reset the DRAM timing defaults to the slowest case and the BIOS then optimises timing for the best performance. DRAM of 70ns or faster should be used.

Note that only the first 640k bytes of DRAM are usually directly accessible by DOS. Some of the remaining DRAM is used to shadow the BIOS (see section 6.1) and the remainder is re-mapped above the 1M byte boundary, where it can be used by DOS extenders and by Windows and other operating systems.

The BIOS automatically determines the amount of DRAM present and configures internal FTD4591 registers accordingly.

Memory between C0000H and FFFFFH (the top of the 1M byte block) can be used to shadow BIOS code. This allows the BIOSes to run at the fast DRAM speed rather than the slow EPROM speed. Typically and the system BIOS (from F0000H - FFFFFH), the VGA BIOS (from C0000H - C7FFFH) and the Flash File System (from C8000H C9FFFH) driver are shadowed. Memory beyond the 1M byte limit is available for Windows and other protected mode operating systems.

## 2.4 FLASH MEMORY

A 1M byte Flash memory chip is fitted to the TC586. Flash memory is non-volatile memory which can be programmed while it is soldered to the TC586. Data written to the Flash memory is retained after power is removed. The board is also tracked to accept a 2M byte Flash chip as an alternative to the 1M byte part. The 2M byte option is a factory fitted option, and may be subject to minimum order quantities. Ask your distributor for details.

The Flash memory serves two purposes. Firstly, it contains the BIOS machine-dependent software that is required to run an operating system. The BIOS occupies the top 64k of the 1M byte Flash chip. A second 64k bytes of the flash chip can optionally be used to store other “BIOS Extensions” - such as the VGA BIOS, a Flash File System driver and other BIOS extensions. See section 2.5 for more information on memory mapping of the TC586.

The TC586 comes pre-programmed with a system BIOS and a VGA BIOS (for the VGA chip on the TCDEV Development System). See section 6.1 for further details on the BIOS.

The second function of the Flash memory is for users who want a solid state disk. A Flash File System is provided with every TC586. This converts the remaining 896k bytes of the Flash chip into a non-volatile read-write logical disk drive. This Flash disk can contain the MS-DOS operating system as well as your application program. The Flash File System is described in section 6.5.

A Utility program is provided on the TC586-UTILS Utility Disk which allows the Flash chip to be programmed by the user. This allows the user to program various alternative BIOS image files into the Flash memory. This utility program is described in section 6.3.

The TC586 is normally supplied with a 1M byte Intel 28F008 flash chip. This chip requires a +12V programming voltage called Vpp, and so an on-board Vpp generator has been provided. The TC586 can also accommodate the AMD 29F080, which is also a 1M byte chip but which does not require a +12V Vpp. The board is also tracked to accept a 2M byte flash chip, the AMD 29F016. (Note that the Flash memory must be fitted during the manufacturing process, so a minimum order quantity may apply for boards with 2M bytes of Flash. Contact your distributor for details if you need this extra Flash memory.

The TC586 allows the Flash File System to access the large Flash chip through a small (16k byte) window in the 1M byte address space. DSP Design have added bank switching logic to the TC586 to achieve this. The high order address lines (A14-A20) of the Flash chip can be changed by software. The Utility Register controls these address pins (see section 3.11). The Flash File System driver software uses the bank switch logic transparently to the user’s software. Most users will therefore not need to know the details of the operation of the bank switch logic.

A ROMdisk driver may be available for users who are not using MS-DOS style operating systems. This can be of use for QNX users for example.

The Flash chip resides on the eight-bit PC/104 data bus. The FTD4591 chip converts a 32-bit processor access to four eight bit accesses to the Flash chip.

The BIOS makes use of “shadow RAM” in place of the Flash chip for greater speed. In this scheme the BIOS contained within the Flash chip is copied by the BIOS to DRAM at the same addresses. The Flash chip is then disabled and the BIOS is executed from the 32-bit wide DRAM, much faster than it would be from the Flash chip. The system BIOS is shadowed, and any BIOS extension code, such as a VGA BIOS and the Flash File System BIOS Extension, are, also shadowed. BIOS Extensions which may reside on other PC/104 modules (such as VGA boards or LAN boards) may also be shadowed: this shadowing is enabled or disabled by the Setup menu.

## 2.5 MEMORY ADDRESS MAP

Table 2 below shows the memory map as configured by the standard BIOS EPROM of the TC586. This table shows the bottom 1M byte address space. Extra DRAM is located immediately above the 1M byte boundary. Note that at the time of writing the memory area from E0000h - EFFFFH is used by the BIOS during its boot sequence, and is then made available for PC/104 bus boards. However, if PC/104 bus boards are present at E0000h - EFFFFH they are

liable to interfere with the boot process. It may be that in the future a BIOS will become available which does not use any of the E0000h region. Contact DSP Design if you really must use memory mapped devices at E0000h.

| Address | Memory Device Decoded | Size |
|---|---|---|
| FFFFF F0000 | BIOS in Flash Chip<br>Copied to shadow DRAM during boot sequence | 64K |
| EFFFF E0000 | Some of this space is currently used by the BIOS during boot sequence, after which, it becomes free. Available for PC/104 memory mapped boards. | 64K |
| DFFFF D0000 | Available for PC/104 memory mapped boards. BIOS Extension code can be located here and optionally shadowed in DRAM. | 64K |
| CFFF CC00 | Reserved for flash File System and Flash Programming program. PC/104 boards should not use these addresses. | 16K |
| CBFFF C8000 | Available on the PC/104 bus. BIOS Extension codecan be located here and optionally shadowed to DRAM. BIOS Extension code contained in the Flash memory (.e.g the FFS driver) can be shadowed to DRAM at this address. | 16K |
| C7FFF C0000 | Usually the VGA BIOS, which is normally copied from Flash chip to shadow DRAM at this address. Alternatively used by VGA BIOS on PC/104 bus which can be shadowed. | 32K |
| BFFFF A0000 | Usually allocated to VGA memory. | 128K |
| 9FFFF 00000 | DRAM | 640K |

Table 2: TC586 Address Map - First 1MByte

## 3 PERIPHERALS

This section describes the I/O address map and the on-board peripherals.

### 3.1 I/O ADDRESS MAP

The TC586 features a number of on-board I/O mapped resources, and supports access to the PC/104 bus I/O space as well.

All I/O mapped functions which are present on the IBM PC/AT are present at the same I/O addresses on the TC586. The TC586 is therefore compatible at the machine code or register level with the IBM PC/AT.

On-board I/O devices include registers within the FTD4591 chip and registers in the Super I/O chip. The Super I/O chip contains the Utility Register, keyboard controller, calendar/clock module and the serial and parallel I/O modules. The on-board I/O addresses are listed in Table 3.

Those addresses which are not on-board are available for peripheral devices on the PC/104 bus. I/O addressing of PC/104 bus boards is reasonably straightforward: if an I/O address is not used by on-board resources then it can be allocated to a PC/104 board. Putting this another way, the addresses of PC/104 bus boards should be chosen to avoid the on-board I/O resources. Note that, in common with many ISA bus I/O boards, PC/104 address decoding logic

often decodes on address lines A0 - A9, which can result in “aliasing” - whereby a PC/104 board can respond to more than one address. For example, a PC/104 bus board set for I/O address 200h may also respond at I/O addresses 600h, A00h, E00h and so on.

| Address | I/O Function |
|---|---|
| 000 - 00F | DMA Controller in FTD4591 |
| 020 - 021 | Interrupt Unit in FTD4591 |
| 022 | Internal Configuration Index Register - Cyrix CPUs |
| 023 | Internal Configuration Data Register - Cyrix CPUs |
| 02E - 02F | Super I/O Chip Configuration Registers |
| 040 - 043 | Timer Unit in FTD4591 |
| 061 | Port B Control/Status Port in FTD4591 |
| 062 - 064 | Keyboard Controller in Super I/O chip |
| 070 - 071 | RTClock in Super I/O chip & NMI enable in FTD4591 |
| 092 | Port A Control/Status Port in FTD4591 |
| 078 - 079 | Utility Register in Super I/O chip |
| 080 - 08F | DMA Page Registers in FTD4591 |
| 0A0 - 0A1 | Interrupt Control/Status Register in FTD4591 |
| 0C0 - 0DF | DMA Controller in FTD4591 |
| 2F8 - 2FF | COM2 Serial port in Super I/O chip |
| 378 - 37A | Parallel Port in Super I/O chip |
| 3F8 - 3FF | COM1 Serial Port in Super I/O chip |
| FC22 - FC2F | FTD4591 Internal Configuration Registers |

Table 3: On-Board I/O Addresses

Note: Registers in the FTD4591 chip in the address range 00 - FF, marked *, are aliased every 1K bytes.

### 3.2 SPEAKER

A PC compatible loudspeaker port is implemented on the TC586. This allows for production of tones, tunes, keyboard clicks etc. PC software which generates sound will therefore operate as expected with the TC586. The TCDEV has a small loudspeaker mounted to it and connection is made to the TC586 via the J3 I/O cable assembly. External speakers should be connected between the J3 signal called SPKR and VCC (+5V).

### 3.3 SERIAL PORTS

The TC586 features two RS-232 serial ports which are accessed as COM1 and COM2. Additionally the COM2 port can be configured for RS-485 operation. The serial ports are fully hardware and software compatible with the IBM PC/AT serial ports and all PC communications software packages will work with the serial ports. The UARTs are 16C550 compatible and thus provide a 16 byte transmit and receive FIFOs. The UARTs are contained within the PC87306 Super I/O chip.

Connection is made to the serial ports via the 50-way J3 connector. If you are using a TCDEV the serial ports are available through the standard 9 pin D-Type connectors at J4 (COM1) and J5 (COM2). These connectors are pin compatible with IBM AT computers.

The serial ports provide the full complement of RS-232 signals. Transmit Data, Request To Send (RTS) and Data Terminal Ready (DTR) are outputs from the TC586. Receive Data, Data Carrier Detect (DCD), Data Set Ready (DSR), Clear to Send (CTS) and Ring Indicator (RI) are inputs to the TC586.

Following a reset of the TC586 the COM1 serial port is initialized as 2400 baud, one stop bit, seven data bits and even parity. These parameters can be changed by the MS-DOS MODE command.
COM1 serial port uses interrupt level IRQ4 to interrupt the processor. The COM2 serial port uses interrupt level IRQ3. It should be noted that the BIOS does not make use of serial port interrupts, but that most comms software packages enable the interrupts and make use of them to increase the speed of serial data transfer. DSP Design is able to supply an interrupt driven communication package called COMMDOS-DRV ask for details.

As an option COM2 can be re-configured as an RS-485 serial port. The COM2 RS-485 port configuration provides a half duplex single twisted pair serial interface. In half duplex mode several boards are connected to the single twisted pair, with no more than one board driving the cable at once. A suitable protocol needs to be agreed by all nodes on the twisted pair to ensure that only one computer transmits at any one time.

On the TC586 the RS-485 driver is controlled by the RTS bit of the on-board UART. When RTS is off (inactive) the RS-485 transceiver does not drive the twisted pair cable. This is the default state after a TC586 reset. When RTS is set active the RS-485 transceiver drives the twisted pair cable and the TC586 can transmit. Note that the receiver part of the transceiver is always enabled, even when it is transmitting, so that COM2 will receive the characters that it transmits itself.

In RS-485 mode the DTR control output has no effect, and the CTS, DCD, DSR and RI status inputs are undefined (they can be in either state, and software must not assume any particular values of these signals).

No RS-485 termination resistors are provided on the TC586. These must be provided externally if required.

The COM2 serial port can be converted to RS-485 operation as described in Appendix B.

The COM2 serial port can also be configured to operate as an IRDA-compatible infrared serial comms port. The IRDA standard defines a number of protocols. The TC586 supports the SIR format, with speeds of up to 115k baud. The IRDA transmit and receive data signals are available on the 50-way I/O connector J3 pins 1 and 2, from where they can be connected to an IRDA infrared transceiver module. Note that these pins are accessible on the TC-DEV Development System at jumper area E1. (The REV B TC586 does not support IRDA operation).

To configure the serial port as an IRDA port you must use the Peripheral menu item within the SETUP program (see section 6.1 for details of the SETUP program).

The serial ports can be individually disabled by software, and there is some control over the addresses they can be assigned. This is done using the SETUP program following a reset of the TC586. The Peripherals menu item within the SETUP program allows this control over the serial ports. Users should exercise care when making changes using SETUP. See section 6.1 for details of SETUP.

### 3.4 CENTRONICS PRINTER PORT

The TC586 implements a full-function Centronics compatible printer port. This port is the MS-DOS PRN device. The Centronics port is contained within the PC87306 Super I/O chip.

The Centronics port features an 8-bit data port and the full compliment of control signals - four output signals and five input signals.

The I/O signals on the printer port can be treated as general purpose digital input and output signals, and as such can be used for other applications (such as driving a small LCD display, for example).

The 8-bit data port is normally used as an output port for driving a printer. It can be used as an input port however. The default setting (after reset) is output. To configure as an input bit 5 of the printer port Control Register must be set to 1. To re-configure as an output set bit 5 to 0. The Control Register is a read/write register located at address 37AH.

The Centronics port signals are brought out on the 50-way J3 I/O connector on the TC586. On the TCDEV the parallel port is accessed via a PC compatible 25 way female D-type connector.

The parallel port is able to use interrupt IRQ7 to interrupt the processor. Users should note that the BIOS does not make use of interrupts for accessing the printer port, but other software drivers may do so. If it is not used by the printer software then IRQ7 can be can be allocated to the PC/104 bus.

The printer port can be disabled by software, and there is some control over the address it can be assigned. This is done using the SETUP program following a reset of the EC586. The Peripherals menu item within the SETUP program allows this control over the printer port. Users should exercise care when making changes using SETUP. See section 6.1 for details of SETUP.

The printer port can optionally be configured as an Enhanced Parallel Port (EPP) and as an Extended Capabilities Printer Port (ECP). In EPP mode greater throughput is provided by automatically generating strobe signals. In ECP mode a 16-byte FIFO Is provided and data transfer under DMA control is possible. Users must provide their own software for these modes. The parallel port mode can be set with the SETUP program - see section 6.1 for details of SETUP.

### 3.5 CALENDAR CLOCK CHIP

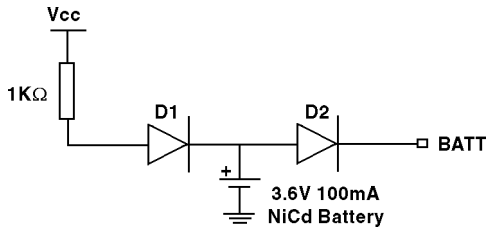
Calendar/clock functions are implemented within the FTD4591 chip. These functions emulate those found in the Motorola MC146818 chip. This chip provides time of day functions, calendar functions and CMOS RAM for storing setup parameters. An alarm facility is also provided; this allows an interrupt to be generated when a particular time is reached.

The calendar/clock chip may be accessed through the MS-DOS calls (interrupt 1AH) or with MS-DOS TIME and DATE commands. As well as the calendar clock functions there are 242 bytes of static RAM which are backed up by the battery. This is used to store configuration parameters used by the BIOS. The serial EEPROM can be used to store these parameters in systems which have no battery - see section 3.1 0 for details.

A battery can be used to provide power to maintain the clock and CMOS RAM when the main power is not present. This external battery should be connected between the BATT input and GND of J3. The battery voltage should be between 3.6V and 5V and can be either be a rechargeable battery (e.g. Nicad) or a non-rechargeable battery (e.g. Lithium).
The FTD4591 chip draws approximately l0µA from the battery when the TC586 is powered down and draws no current when operating normally (i.e. powered up).

The TCDEV has a 3.6V 100mAhr Nicad rechargeable battery installed. This connects to the BATT input via an enable/disable jumper, as described in the TCDEV manual. It is estimated that the TCDEV Nicad battery should be sufficient for the clock to operate for several months in the absence of the +5V power supply. The jumper E2 is provided on the TCDEV which can be used to disconnect the battery in order to extend the battery life. The battery should be disconnected while the TC586/TCDEV is in storage.

Figure 2 gives a suitable circuit for a rechargeable battery back-up circuit.




NOTE: The circuit shown above is identical to the circuit used on the TCDEV. This circuit is suitable only when using a Nicad battery of the type used on the TCDEV. The circuit shown in figure 2 is not suitable for Lithium or other battery types. Diode D1 and the resistor must be omitted if a lithium battery is used.

Figure 2 - Recommended Battery Back-up Circuit

### 3.6 FLOPPY DISK DRIVE

Users who require a floppy drive can use the TCDEV or TSYST boards manufactured by DSP Design. The TSYST is a PC/104 board which provides floppy, IDE, serial and parallel interfaces. The TCDEV incorporates a complete floppy system, including a floppy diskette drive and cable. Connection to the TC586 is via the PC/104 bus.

### 3.7 IDE DISK DRIVE

Users who require an IDE hard drive can use the TCDEV or TSYST boards manufactured by DSP Design.

The TCDEV incorporates an IDE controller and standard 2½ IDE drive connector. Your supplier can supply 2½" IDE disk drives. These can be mounted to the TCDEV to give a complete hard disk solution. A 2½ inch to 3½ inch IDE drive converter cable is available which allows 3½ inch hard disk drives to be connected to the TCDEV (a separate PSU is required for the 3½ inch drive in this configuration). The converter cable is called the IDE3020.

The TSYST is a PC/104 board which provides floppy, IDE, serial and parallel interfaces. It accepts 3½ inch hard drives as standard and can be interfaced to a 2½ inch drive using the IDE3020 cable assembly.

### 3.8 VGA GRAPHICS

Users who require VGA graphics can use the TCDEV or TV750 boards manufactured by DSP Design. The TCDEV incorporates a simple VGA system including a standard 15 pin VGA connector for easy connection to VGA monitors. Connection to the TC586 is via the PC/104 bus.

The TV750 is a PC/104 format board and is a high performance VGA controller available with up to 1Mbyte of video memory. It can drive CRT displays and a wide range of flat panels including passive STN and active-matrix TFT LCDS, EL and plasma panels.

### 3.9 KEYBOARD AND MOUSE

The TC586 uses an AT type keyboard, as opposed to the XT type. Many keyboards operate in both modes and have a switch to select PC/XT or AT operation. Your supplier can provide a suitable keyboard.

In many applications the familiar desktop keyboard is inappropriate. A variety of industrial keyboards and keypads are available - contact your dealer or DSP Design for details. DSP Design suggest that you avoid the keypad encoders from Keymat Technologies as we have had problems with noise with these keyboard encoders. The TC586 will work without a keyboard if required.

Users should avoid plugging in the keyboard or mouse when the TC586 is powered on.

The keyboard controller circuitry on the TC586 is contained within the Super I/O chip, and also includes a PS/2 style mouse port. The keyboard uses the IRQ1 interrupt line and the mouse uses IRQ12. Connections to the keyboard and mouse are made through the 50-way J3 connector. If you are using the TCDEV the keyboard and mouse are accessible through the J8 mouse port connector (PS/2 style) and the J7 AT keyboard connector.

### 3.10 SERIAL EEPROM

The TC586 has a serial EEPROM chip fitted. This is used primarily to store set-up parameters in systems which lack a battery to retain this data in the CMOS RAM. There is some space available in the serial EEPROM for users' data. The serial EEPROM chip also contains the watchdog timer, which is also accessed through the serial interface.

See section 6.5 and 6.6 for information on using the serial EEPROM utility programs.

### 3.11 UTILITY REGISTER

The TC586 has a Utility Register which controls a number of peripheral functions including the Flash memory bank switching, Vpp generator and serial EEPROM interface. The Utility Register is located within the PC87306 Super I/O chip and appears in the I/O address space. The Utility Register occupies two 8-bit I/O locations at addresses 0ECh - 0EDh.

The Utility Register is used extensively by the flash File System driver software and the serial EEPROM software, and will to normally be accessed by the user.

Table 4 gives the function of each bit in the Utility Register. Following reset all bits are set to logic 1. They have internal pull-up resistors fitted, and can be set to 0 by writing a 0 to the Utility Register or if an external device (e.g. the serial EEPROM) pulls a pin to 0. The registers are read-write. When writing to the registers the user should read the current state, change only the required bits, and write the results back. Users should not change bits they do not understand, or the TC586 may stop working.

Note that bit 3 of the port at 0EChh differs between REV B and REV C. REV B boards can be identified by the text “176001.B00” on the PCB copper, underneath the DIMM memory module. REV C boards have “176001.C00” in this position.

## 4 PC/104 BUS AND STAND-ALONE OPERATION

The TC586 will operate as a stand-alone single board computer, or it can use the PC/104 bus interface to expand its capabilities with the wide range of PC/104 bus I/O cards currently available. This section of the manual describes first the stand alone operation and then operation on the PC/104 bus.

| Bit | Port | Function | |
|---|---|---|---|
| 0 | ECh | DRIVEA16- | For Flash memory programming |
| 1 | | WRFLASH- | |
| 2 | | ENFLASH- | |
| 3 | | VPPEN (rev B only) | |
| | | A19LOW- (rev C only) | Takes SA19 low on PC/104 bus |
| 4 | | /CS | To serial EEPROM |
| 5 | | SK | |
| 6 | | SI | |
| 7 | | SO | |
| 0 | EDh | BA14 | To Flash memory chip |
| 1 | | BA15 | |
| 2 | | BA16 | |
| 3 | | BA17 | |
| 4 | | BA18 | |
| 5 | | BA19 | |
| 6 | | BA20 | |
| 7 | | SLOWCLK- | |

Table 4: Utility Register Bit allocations

### 4.1 STAND-ALONE OPERATION

The TC586 will operate as a single board computer with the addition of the appropriate peripherals and a single +5V power supply. In stand-alone operation the TC586 need not be plugged into a bus.

The TC586 requires a +5V power supply. Power can be supplied in one of two ways.

The PC/104 bus connectors have various +5V and GND pins available. See Appendix E for actual pin numbers. Some or all of these pins can be connected in parallel and the resulting +5V and GND connected to the power supply. The second option is to use the alternate power connector J4. This is a four pin right-angle Molex socket. +5V and GND should be connected to J4 using a suitable mating connector. See Appendix E for pin assignments and connector part numbers.

Users should take care to provide power to the TC586 through cables which are as short and thick as possible. This is to reduce the voltage drop which will occur through the resistance of the cables.

### 4.2 PC/104 BUS

The PC/104 interface is via the J1 and J2 connectors along the bottom edge of the TC586. The 64-way J1 connector provides the 8-bit data bus and the 40-way J2 connector provides the 16-bit signals. The TC586 is able to interface with both the 8-bit and 16-bit modules that meet the PC/104 specification.

The TC586 is PC/104 compliant. That is, the TC586 conforms to both the electrical and mechanical specifications laid down by the PC/104 V2.3 document. The TC586 is able to interface with both the 8-bit and 16-bit modules that meet the PC/104 specification.

The TC586 complies with the mechanical aspects of the PC/104 V2.3 specification. This includes the use of polarizing pins on the J1 and J2 connectors. Some earlier versions of the PC/104 specification did not use polarizing pins and it was seen that this could result in possible misalignment and subsequent product failure if power was applied before the error was discovered. “Key” positions have been assigned to the J1 and J2 connectors. These can be seen on the J1 and J2 pin assignment diagrams detailed in Appendix E. The key positions have had their pin removed and the socket hole has been blocked to prevent entry by any adjacent pin.

Users should note that any boards produced to PC/104 specifications prior to V2.2 may not mate with V2.2 or V2.3 boards. Prior to the V2.2 specification the key positions were not present, and J2 could have been a right angled connector. The V2.2 and V2.3 specifications do not allow the right-angled J2 connector. Both J1 and J2 on the TC586 are mounted vertically.

10KΩ pull up resistors have been added to the SD0 - SD15 data bus signals. There are pull-up resistors of approximately 50KΩ on the /IOCHCHK and all IRQ signals on the PC/104 bus. The IOCHRDY, /IOCS16, /MEMCS16 and /ZEROWS signals have 330Ω pull up resistors on the PC/104 bus. The DREQ0 - DREQ7 signals have 10KΩ pulldown resistors.

### 4.3 CLOCK AND RESET SIGNALS

Two PC/104 clocks are provided: the bus clock (BUSCLK) and an asynchronous oscillator (OSC). The OSC signal is a clock running at 14.3181 MHz. The PC bus clock normally runs at 1/4 of the processor clock, but can be altered by using the TC586 BIOS Setup utility (see section 6.1 for details). Note however that entering the “Advance Chipset Setup” menu of the BIOS Setup program causes the BIOS to autosense the processor local bus speed and then to set the BUSCLK frequency to a speed closer to 8MHz. These speeds and the corresponding clock divisor is given in Table 5.

| Local Bus Clock Frequency | Following Reset | | After Reset | |
|---|---|---|---|---|
| | BUSCLK | Divisor | BUSCLK | Divisor |
| 25MHz | 6.25MHz | 4 | 8.33MHz | 3 |
| 33MHz | 8.25MHz | 4 | 8.25MHz | 4 |
| 40MHz | 10.0MHz | 4 | 8.0MHz | 5 |

Table 5: BUSCLK Frequency

The TC586 can reset the PC/104 bus. See section 5 for details. The TC586 drives the PC bus RESETDRV signal but cannot be reset by the RESETDRV signal.

The TC586 can be reset by issuing a low going pulse on the /RESET line of the J3 connector. The TC586 will then force the RESETDRV signal of the PC/104 bus to be driven. In this way a system reset can be generated by an external signal or switch. The TCDEV has a push button switch connected between /RESET and GND. Pressing this switch momentarily will reset the system.

### 4.4 INTERRUPTS

The following interrupt signals are connected directly from the PC/104 bus to the FTD4591 chip: IRQ9 (IRQ2), IRQ3 to IRQ7, IRQ10, IRQ11, IRQ14, IRQ15 and /IOCHCK (which is a non-maskable interrupt). If any interrupts are used by the on-board peripherals then they are not available for use by a PC/104 bus card. Note that IRQ4, IRQ3, IRQ6 and IRQ7 are normally allocated to COM1, COM2, the floppy disk drive and the printer port respectively. These may be available for PC/104 peripherals if they are not being used by these on-board peripherals, although this may also depend on whether your operating system will release these for general purpose interrupts.

### 4.5 DMA

The following DMA signals are available on the PC/104 bus: DREQ0 - DREQ3 and /DACK0 - /DACK3 are used for eight bit transfers. DREQ5 - DREQ7 and /DACK5 /DACK7 are used for 16 bit transfers. The TC signal is a Terminal Count indicator. The bus master facility (using the /MASTER signal) is not supported on the TC586.

## 5· RESET OPTIONS

A full set of reset options exist for the TC586. The reset circuit is built around the X25043 serial EEPROM chip, which provides reset functions as well as memory. This chip includes a power supply monitor and a watchdog timer. To avoid glitches on the reset signal the X25043 will always hold the reset signal asserted for approximately 200ms. This ensures all circuitry is property reset, and conforms to the PC bus specification.

The X25043 resets the FTD4591 chip, and also the PC/104 bus by driving the RESETDRV signal high.

### 5.1 POWER SUPPLY MONITOR

The X25043 monitors the +5V supply voltage. When the supply drops below about 4.5V the X25043 will assert the TC586 reset signal. Once the power supply returns to being within specification, the reset signal will be released after 200ms. This circuit prevents power “brown-out” causing unpredictable behaviour.

Users should note that if the voltage drop across the cables which link the power supply to the TC586 is excessive then the power supply monitor may reset the TC586. This may also happen if there are noise spikes on the power supply. It is recommended that all power supply cables be as thick and short as possible to minimize the voltage drop across them.

### 5.2 ON-BOARD WATCHDOG TIMER

A watchdog timer exists on the X25043. The function of a watchdog timer is to reset a computer if the software has crashed. The correct operation of the timer relies on software to access the watchdog timer hardware on a regular basis. If the software crashes, the watchdog timer will not be “kicked” and so eventually it will time-out and reset the computer. The watchdog timer function is accessed via the Utility Register.

The Utility Register is a multi-function register which among other things gives access to the four control signals on the X25043 serial EEPROM. The Utility Register is described in section 3.1 1. The watchdog is enabled by writing an

enable command to the X25043 via the Utility Register. Once this has been initiated, an internal clock to the X25043 starts counting and will continue to count until it times out, until the watchdog timer is "kicked" by the user's application software, or until the watchdog timer is disabled by a disable command sent to the X25043.

The watchdog timer period can be set to approximately 1.4s, 600ms. or 200ms, or it can be disabled. Once it has been enabled the watchdog timer must be accessed repeatedly by the user's software. If the watchdog timer is allowed to time out the X25043 chip will issue a hardware rest to the TC586 (and to the PC/104 bus).

The watchdog timer is "kicked" by taking its chip select (/CS) pin low then high. The /CS pin is driven by bit 4 of the Utility Register at I/O address 0ECh. The TC586-UTILS utility disk has documented sample code illustrating the use of the watchdog function. Note that it is the responsibility of the user to design code which will reliably kick the watchdog timer.

The BIOS includes code which disables the watchdog timer immediately after a reset, and thus if a watchdog time-out occurs the watchdog timer is disabled until after the operating system is loaded and the application software re-enables it. See section 6.7 for further information on the watchdog timer.

### 5.3 RESET SWITCH

A reset switch or similar can be connected to the TC586 via the 50-way J3 I/O connector. The reset switch connects between J3 pins 23 and 24. (Pin 24 is the /RESET input, and pin 23 is a GND pin). See section 4.3 for more details. The reset switch on the TC-DEV is connected in this fashion.

### 5.4 RESETTING THE PC/104 BUS

The TC586 always resets the PC/104 bus via the RESETDRV signal. The active high RESETDRV signal is asserted whenever the X25043 is driving the TC586 on-board reset signal - that is, in response to a power failure, watchdog timer time-out, or a low going pulse on the /RESET line of the J3 I/O connector.

It is not possible to reset the TC586 by driving the RESETDRV signal on the PC/104 bus.

## 6 SOFTWARE

The TC586 offers a very high degree of PC compatibility. The vast majority of software (both operating systems and applications software) which will run on IBM PC/AT will also run satisfactorily on the TC586.

Most users will wish to use the MS-DOS operating system (booting from a hard disk, floppy disk or ROM-disk) and then run off-the-shelf software, or their own application. DSP Design offers a number of software products to ease software development.

### 6.1 SYSTEM BIOS

The system BIOS is a program which interfaces between the TC586 hardware, the operating system and application code. It is responsible for controlling the TC586 hardware and providing a standard interface to the higher levels of software. The BIOS also deals with functions such as initialization and testing the TC586 hardware following power-on.

The TC586 uses a system BIOS supplied by AMI. Users should note that the BIOS is the copyright of AMI.

The BIOS has an inbuilt Setup program, which can be invoked by typing the DEL key at the keyboard during the boot sequence. The setup program allows many system parameters to be changed, and then stored in CMOS memory. Amongst the parameters which can be changed are the current time and date, disk drive types, enabling and disabling and address selection of peripheral devices, BIOS shadowing and AT bus clock speed.

The serial and parallel ports can be enabled or disabled by the Setup program, and their I/O addresses can be changed. This could be required to allow the TC586 to coexist with other PC/104 boards which are already using the standard COM1, COM2 and PRN I/O addresses. The serial and parallel devices are configured in the Peripheral Setup menu.

The Setup Utility is menu driven, and its operation should be self-explanatory. Users must not change parameters which they do not understand.
Setup parameters are stored in the on-board CMOS memory, and it is backed-up if an external battery is provided. If no external battery is present then the Setup parameters can be stored in an on-board serial EEPROM, as described in section 6.6.

The BIOS is programmed into the Flash memory chip as part of the manufacturing process. Note that the BIOS and BIOS extensions are combined in a single 128k byte file, which is programmed into the top 128k bytes of the Flash memory chip. The Flash memory chip can be changed by the user if necessary, as described in section 6.4. The default is for a system BIOS, the TC-DEV VGA BIOS extension and the Flash File System BIOS Extension to be programmed into the Flash memory.

A number of pre-configured BIOS files are available on the TC586-UTILS diskette. These differ in the BIOS extensions which they contain. See the READ.ME file in the BIOS directory of the TC586-UTILS Utility Disk for further details.

Under some circumstances the TC586 BIOS may need to be modified or additional BIOS code may need to be added to the BIOS EPROM. Tools exist to deal with these issues, so contact your dealer for details.

### 6.2 VGA BIOS AND OTHER BIOS EXTENSIONS

As well as the system BIOS, the Flash memory chip can contain other BIOS extensions. These include the VGA BIOS and the Flash File System BIOS.

#### 6.2.1 PRINCIPLES OF OPERATION

The system BIOS and the BIOS extensions are combined into a single 128k byte file, which is programmed into the Flash memory chip using a Flash programming utility, as described in section 6.4. A number of these pre-configured BIOS image files are present on the TC586 Utilities Disk. The pre-configured files include options with and without the TCDEV VGA BIOS, and with and without the Flash File System driver.

If these pre-configured BIOS image files are not suitable, (for example if other BIOS extensions must be copied into the Flash memory) then a utility program is available for generating new 128k byte BIOS image files. This program is called AMIEMBED.EXE, and is provided on the TC586 Utilities Disk. A README.TXT file on the disk describes the operation of this program.

As well as executing BIOS extensions contained within the Flash chip, the BIOS also searches the PC/104 bus for BIOS extension EPROMs which might be present in the system. If valid BIOS extension EPROMs are found on the PC/104 bus then they are executed.

There is a special case relating to VGA BIOS extensions. Before the TC586 BIOS installs a VGA BIOS from within the Flash chip it first examines the PC/104 bus, looking for any other VGA BIOS which may be present. If another VGA BIOS exists (because the user is using another VGA controller such as DSP Design's TV750, for instance) then this other VGA BIOS is used and the VGA BIOS in the Flash chip is not used. This can be a useful feature if more than one VGA board is used in a system.

#### 6.2.2 THE VGA BIOS EXTENSION ON STANDARD TC586 BOARDS

The TC586 boards include two BIOS extensions. One is for the 65535 VGA controller chip found on TCDEV development systems of REV D and later. The second BIOS extension is the Flash File System BIOS extension.

The VGA BIOS programmed in the TC586 will also work with the VG-660 VGA controller on REV B TCDEV development systems.

Users will find that when the TC586 is removed from the TCDEV the VGA BIOS will beep several times, indicating that it cannot find a VGA controller chip. You may wish to reprogram the flash memory with a BIOS image which does not contain a VGA BIOS.

If the TC586 lacks a VGA BIOS it will still work with the revision D or later TCDEV boards, since these boards contain their own on-board VGA BIOS. To enable the onboard VGA BIOS fit a jumper in the EN position at C000h for jumper area E6. However a TC586 without a VGA BIOS will not work with a revision B TCDEV.

### 6.2.3 FLASH FILE SYSTEM BIOS EXTENSION ON STANDARD TC586

The standard TC586 bios includes two BIOS extensions. One is for the 65535 VGA controller chip found on TCDEV development systems of REV D and later. The second BIOS extension is the Flash File System BIOS extension.

The Flash File System BIOS allows the remaining flash memory to be configured as a disk drive. This is described in section 6.5.

The Flash File System driver will cause the Windows 95 disk system to run slower. This is because when the Flash File System is installed Windows 95 uses the 16-bit DOS file system, rather than its faster 32-bit native file system. It is unlikely that Windows 95 users will want to use the Flash File System, so these users should reprogram their Flash memory with a BIOS image without the Flash File System. A suitable BIOS image exists on the TC586 Utilities Disk.

It is likely that the Flash File System BIOS extension will not operate with some other operating systems, and may need to be removed.if the Flash chip is not used. This can be a useful feature if more than one VGA board can be used in a system.

## 6.3 MS-DOS AND OTHER OPERATING SYSTEMS

The TC586 will run any version of MS-DOS, and should run any other operating system which will run on a PC. The computer will boot MS-DOS from a floppy disk, from a hard disk or from the Flash File System.

DSP Design supply Microsoft's MS-DOS operating system. Users should note that most copies of MS-DOS obtained from other sources may not legally be run on the TC586 under the terms of the Microsoft license agreement. Bootleg copies of the operating system of course may not be run on the TC586.

Any other operating system which will run on a 386 or 486 based desk top computer should also run on the TC586. For example Windows has been successfully tested on the TC586.

## 6.4 FLASH MEMORY PROGRAMMING

Flash programming utility programs provide facilities for programming data into the Flash memory chip on the TC586. The programs can erase some or all of the Flash chip, and can write a file from disk to the Flash chip.

There are two Flash programming programs - TC5F008.EXE is for the Intel 28F008 Flash chip (shipped on the standard TC586) and TC5F016.EXE is for the Fujitsu or AMD 29FO16 Flash chip which can optionally be fitted.

The Flash programming utility is normally used to write a new BIOS to the Flash memory. It is not required to create the Flash File System disk in the Flash chip.

### 6.4.1 PROGRAMMING THE 28F008

The following describes the process of programming the Intel 28F008 chip, which is the Flash chip installed as standard on the TC586.

The 28F008 flash device is arranged as 16 sectors of 64k bytes each. Each block is erased separately, and it is not possible to erase less than 64k bytes at a time. The TC5F008.EXE programming utility is used to program the 28F008 device is available on the TC586-UTILS Utility Disk. It is run with the following parameters:

The program can be run in two ways - most commonly to safely program a BIOS image file into the Flash chip, and also in a more flexible way, to allow any file to be programmed at any location in the Flash chip.

In the safe BIOS programming mode TC5F008 is run with the following single parameter:-

TC5F008 -u<filename>

-u u for "update BIOS". Program the specified BIOS image file into the device. In this safe mode the program checks to see if the file is present on the disk, and is a plausible BIOS image (ie. it is 128K bytes in length). The program then erases the top 128K bytes of the Flash memory, and then programs with verify, the file.

In the flexible mode TC5F008 is run with any or all the following parameters:-

TC5F008 -e -sx -p<filename> -v<filename> -oxxxxx -lxxxxx -q -dxxxxx -h

-e If -e is specified the entire device will be erased. If -e is not specified the device will not be erased. The default is to not erase.

-sx If -sx is specified then the sector specified by x is erased. The value for x is a hexadecimal digit between 0 and F.

-p -p<filename> program the specified file into the device. This parameter defaults to “do not program”.

-v -V<filename> verifies the contents of the flash device against the data in the file specified by <filename>. If the chip and the file differ the address of the first byte which differs is printed, together with the values of the differing bytes. The default is not to verify.

-0 -oxxxxx. Start programming the file at this offset from the start of the flash device. xxxxx is a 20 bit (5 hex digit) hexadecimal number. This parameter defaults to 0. For programming the 128k byte BIOS image file you should use the parameter -oE0000.

-l -lxxxxx. This is the maximum number of bytes of data to program into the Flash chip. The number of bytes programmed will be the either the file length or the number of bytes specified by this parameter, whichever is the smaller. This parameter defaults to the size of the Flash device (100000h bytes in the case of the 28F008).

-q Quiet. This parameter minimizes screen output. The default is “not quiet”.

-d -dxxxxx. This option displays the contents of the Flash chip at the 20-bit (5 hex digit) hexadecimal address xxxxx. The output is 16 lines each of 16 hex bytes. The default is not to print data.

-b Use this option only if you are programming a REV B TC586.

-h Displays a help menu.

The TC5F008.EXE program can be used to write one or more files to the Flash chip, by running the program several times with different -p, -s and -o options each time.

### 6.4.2 PROGRAMMING THE 29F016

The following describes the process of programming the AMD or Fujitsu 29F016 chip. Note that the chip installed on the standard TC586 is the Intel 28F008.

The 29F016 flash device is arranged as 32 sectors of 64K buyes each. Each block is erased separately, and it is not possible to erase less than 64K bytes at a time. The TC5F016.exe programming utility is used to program the 29F016 device is available on the TC586-UTILS Utility disk. It is run with the following parameters:-

In the safe BIOS programming mode TC5F016 is run with the following single parameter:-

TC5F016 -u<filename>

-u u for "update BIOS". Program the specified BIOS image file into the device. In this safe mode the program checks to see if the file is present on the disk, and is a plausible BIOS image (ie. it is 128K bytes in length). The program then erases the top 128K bytes of the Flash memory, and then programs with verify, the file.

In the flexible mode TC5F016 is run with any or all the following parameters:-

TC5F016 -e -sx -p<filename> -v<filename> -oxxxxx -lxxxxx -q -dxxxxx -h

-e If -e is specified the entire device will be erased. If -e is not specified the device will not be erased. The default is to not erase.

-sx If -sx is specified then the sector specified by x is erased. The value for x is a hexadecimal digit between 0 and 1F.

-p -p<filename> program the specified file into the device. This parameter defaults to “do not program”.

-v -V<filename> verifies the contents of the flash device against the data in the file specified by <filename>. If the chip and the file differ the address of the first byte which differs is printed, together with the values of the differing bytes. The default is not to verify.

-0 -oxxxxx. Start programming the file at this offset from the start of the flash device. xxxxx is a 21 bit (6 hex digit) hexadecimal number. This parameter defaults to 0. For programming the 128k byte BIOS image file you should use the parameter -o1E0000.

-l -lxxxxx. This is the maximum number of bytes of data to program into the Flash chip. The number of bytes programmed will be the either the file length or the number of bytes specified by this parameter, whichever is the smaller. This parameter defaults to the size of the Flash device (200000h bytes in the case of the 29F016).

-q Quiet. This parameter minimizes screen output. The default is “not quiet”.

-d -dxxxxx. This option displays the contents of the Flash chip at the 21-bit (5 hex digit) hexadecimal address xxxxx. The output is 16 lines each of 16 hex bytes. The default is not to print data.

-h Displays a help menu.

The TC5F016.EXE program can be used to write one or more files to the Flash chip, by running the program several times with different -p, -s and -o options each time.

### 6.5 FLASH FILE SYSTEM

This section describes the Flash File System.

#### 6.5.1 OVERVIEW

The ability to operate without mechanical disk drives is a key feature of the TC586. To do this you can make use of the Flash File System (FFS) which is provided with every TC586. As well as being more robust than mechanical drives they are also very much faster.

The Flash File System is included on the TC586 Utility Disk. It is licensed from Datalight, who call it CardTrick, and DSP Design have paid a license fee for every standard TC586, so you may copy the Flash File System from the disk for every TC586 you buy. (Some volume users who do not require the FFS may ask for TC586 boards without the license, to reduce costs).

The Flash File System driver is implemented as a BIOS extension or as a loadable device driver. In order to boot from the Flash File System disk drive the BIOS Extension option must be chosen, as a loadable device driver can only be loaded after DOS has booted from another disk (such as a floppy disk). However, the loadable device driver option can be used when another device is the boot device. The loadable device driver is also required during the initial formatting of the Flash disk.

The Flash File System driver is normally implemented as a BIOS extension. This driver must be programmed into the Flash memory, and then it is located every time the TC586 boots. The standard TC586 is shipped with the FFS device driver present in the Flash memory as a BIOS extension.

The loadable device driver requires the driver to be placed on the boot disk, and it is activated by an appropriate entry in the CONFIG.SYS file.

In either case, the FFS driver operates by intercepting calls to the BIOS disk drive subsystem, which uses software interrupt INT13. Calls which are not intended for the FFS are passed through to the BIOS. Calls which are intended for the FFS are performed by the FFS driver.

The FFS BIOS extension requires 16k bytes of memory, from CC000H - CFFFFH. A small amount of RAM within the 640k bytes available to MS-DOS is also used by the FFS.

#### 6.5.2 OPERATION OF THE FLASH FILE SYSTEM

The standard TC586 is shipped from DSP Design with the FFS BIOS Extension installed in the Flash memory, and the Flash disk already formatted. Thus most of this section is for information only, as steps 1 - 6 below have already been performed.

The Flash File System software referred to here is on the TC586-UTILS Utility Disk, in the FFS directory. To operate with a Flash File System, perform the steps below:

1. Check that you have a TC586 with a Datalight CardTrick license sticker applied.

2. Confirm that you have the FFS BIOS extension programmed in the Flash memory along with the system BIOS. If not, suitable BIOS files are present on the TC586-UTILS Utility Disk. (Note that if the Flash disk is not to be the boot disk, the FFS driver can optionally be a loadable device driver, installed on the alternative boot disk - e.g. an IDE hard disk. In this case the BIOS extension should not be included in the Flash memory).

3 Boot your computer from a floppy disk containing the FFS driver in its loadable device driver form and a suitable entry ;in the CONFIG.SYS file. The loadable device driver for the 28F008 Flash chip is FTC5F008.EXE and the corresponding entry in CONFIG.SYS is:

DEVICE=FTC5F008.EXE

The loadable device driver for the 29F016 Flash chip is FTC5F016.EXE and the corresponding entry in CONFIG.SYS is:

DEVICE=FTC5F016.EXE

When the Flash File System driver loads it will display a sign on message to confirm that it has been located. (Note that normally the BIOS Extension form of the FFS device driver is used, but the loadable device driver form must be used the first time the Flash disk is formatted).

4 Before the Flash File System can be used the Flash disk must be formatted, using a dedicated formatting program called DLFMT.EXE. The syntax of the DLFMT program is:

DLFMT <drive> [/C] [/V]

<drive> is the drive letter, usually C:

/C This is an optional parameter, and tells the program to format the drive without prompting the user for input.

/V This is an optional parameter and allows a volume label to be placed on the disk. After a format, the program will prompt the user for a volume name.

· At this point you have a functioning Flash disk, although the disk will not be bootable and will have no files on it.

6 Now the DEVICE=FTC5F008.EXE entry should be removed from the CONFIG.SYS file on the boot disk.

7 Once the Flash disk has been formatted the user can use the DOS SYS command to place DOS on the Flash disk. (Note this step is option, but the operating system must be added if the Flash disk is to be the boot disk). To copy the operating system to the Flash Disk type:

SYS C:

8 At this point the TC586 can be re-booted. If all has gone well the Flash File System BIOS Extension will print a sign-on message and the TC586 will boot DOS from the Flash disk.

The Flash disk will be allocated the drive letter C:. It will be the boot disk (provided that the boot sequence in the Setup utility has C: selected as the boot disk). If IDE drives are included in the system they be allocated the next drive letters - D: and E:.

The Flash File System driver maps 16k byte blocks of the Flash chip into address C000:C000 during each Flash disk access. It should be noted that any modules present on the bus at these addresses will see the PC/104 memory read strobes (/MEMR and /SMEMR) during Flash disk accesses. Addresses C000:C000 - C000:FFFF must therefore not allocated to PC/104 bus devices when using the Flash File System.

### 6.5.3 GARBAGE COLLECTION

The nature of the Flash memory is that it can only be erased in 64k byte blocks. The FFS driver thus has the task of allocating logical disk sectors to physical areas of Flash memory. When files are deleted the FFS driver does not immediately erase the corresponding Flash memory. Instead, it marks that memory as being “garbage”, and when the Flash memory approaches its capacity the FFS performs a garbage collection process, in which data which is still required is copied into a spare 64k byte block, freeing another block to be erased.

As a consequence of the garbage collection process, some writes will take longer than others, if they force the FFS to perform its garbage collection operation. If this is a problem, a program called GARBAGE.EXE can be run, to force garbage collection at any time. The source and executable versions of this program are included on the Utilities Disk.

The FFS also implements a wear-levelling algorithm, to ensure that all parts of the Flash chip are equally used.

## 6.6 SAVING CMOS RAM DATA IN THE SERIAL EEPROM

A serial EEPROM chip on the TC586 provides non-volatile memory storage and also incorporates a watchdog timer. The non-volatile memory can be used to back-up the CMOS SRAM, in systems without batteries, or where the battery may go flat. The serial EEPROM is the Xicor XR25043.

The BIOS includes a feature which checks to see if the contents of the CMOS memory are valid during the boot sequence. If the CMOS memory does not have valid contents (since there was no battery back-up, for instance) then the BIOS will check whether the serial EEPROM contains valid CMOS data. If it does then the data in the serial EEPROM memory will be copied into the CMOS memory.

It is the responsibility of the user to program the serial EEPROM. A utility program is provided to do this. It is called TC5EE.EXE and is available on the TC586-UTILS Utility Disk. It should be run with the -C parameter, like this:

```
TC5EE -C
```

(Note that the TC5EE program has other uses - see 6.7 and 6.8).

The TC5EE program should be run once the CMOS memory contains valid data - after running the BIOS Setup program for instance. The contents of the CMOS registers are then copied into the serial EEPROM. These values will be returned to the CMOS memory by the BIOS if the CMOS memory contains invalid data during subsequent boot operations.

When the TC5EE.EXE program is run all of the first 128 CMOS memory locations are copied to the EEPROM. This includes memory locations which are used by the BIOS, memory locations which are not used by the BIOS, real-time clock and date registers, and the four control registers. The extra 128 memory locations which can be accessed when the MEMSEL bit is set to logic 1 are not copied.

During the restore process, when contents of the serial EEPROM are copied back to the CMOS RAM, all 128 bytes are copied. This restores the time and date, the control registers ans the memory locations containing data.

The BIOS only makes use of some of the CMOS memory locations (in the range 0 - 7Fh), and the others are available to the users for their own purposes. Note that the second 128 bytes of CMOS RAM can only be accessed by setting the RAMSEL bit in the 87306 Super I/O chip to logic 1. The RAMSEL bit acts as a bank select bit, selecting either the standard 128 bytes or the 2nd 128 bytes. Contact DSP design if you need to access the second 128 bytes of CMOS RAM.

Although only some of the CMOS RAM locations are currently used by the BIOS, DSP design strongly recommends that all locations up to and including address 0FFh are reserved for possible future BIOS use. Section 6.7 describes a program which can be used to read and write CMOS SRAM locations.

### 6.7 SERIAL EEPROM PROGRAMMING

Section 6.6 describes using the serial EEPROM for saving CMOS RAM settings. Addresses 100h - 1FFh remain available for users.

The TC5EE.EXE program allows individual bytes in the EEPROM to be written and read. It also provides a way of testing the EEPROM, enabling and testing the watchdog timer, and copying the CMOS SRAM into the EEPROM. It has the following parameters:

TC5EE -rxxx -wxxx -t -c -e -kxxx

-r -rxxx reads the data from the serial EEPROM at the address <xx>, and displays it on the screen. The xxx parameter is a hexadecimal number in the range 0 - 1FFh.

-w -wxxx writes data into the serial EEPROM at the address defined by the <xx> parameter. The data written is the hexdecimal byte specified by the -d parameter. The xxx parameter is a hexadecimal number in the range 0 - 1FFh.

-d -dxx defines the data value to be written to the serial EEPROM by the -w parameter The xxx parameter is a hexadecimal number in the range 0 - 1FFh.

-t -t tests the serial EEPROM, by writing to every location.

-c -c copies the contents of the CMOS SRAM into the serial EEPROM.

-e -e enables the watchdog timer. The TC586 will be reset unless the watchdog is kicked (see the -k parameter).

-k -kxxx kicks the watchdog timer for <xx> seconds. The xxx parameter is a hexadecimal number in the range 0 - 1FFh.

### 6.8 WATCHDOG TIMER PROGRAMMING

The watchdog timer is contained within the serial EEPROM chip and is controlled through four pins of the Utility Register. Once it is enabled, the watchdog timer will reset the TC586 if it is not accessed (or “kicked”) regularly. It is up to the user to write code to enable and kick the watchdog timer. As an example, the source code of a watchdog timer test program is included on the TC586-UTILS Utility Disk. The test program is called TC5WD.EXE.

The general purpose serial EEPROM program, TC5EE.EXE, can also be used to test the watchdog timer - see section 6.7.

The watchdog timer is kicked by the toggling of its chip select pin (/CS), which is driven by the Utility Register bit 4 at I/O address 78h. Users might consider taking the /CS pin low at one point in their program and taking it high again in a different point. This reduces the likelihood that a crashed program could end up executing a small loop which both set and cleared the /CS pin. Similarly, the watchdog accesses should not be part of a timer-based interrupt service routine, since a program could possibly crash and leave a timer interrupt correctly operating.

## APPENDIX A: SPECIFICATION

| | |
|---|---|
| Product: | TC586 |
| Description: | PC/104 format, single board PC compatible computer. |
| Processor: | 80486DX, 80486DX2, 80486DX4 or 5X86 processor. Local bus clock speed selectable as 16MHz, 25MHz, 33MHz or 4OMHz. |
| DRAM: | 4M, 8M or 16M bytes DRAM implemented using 72-pin DIMM memory modules. Provision for 32M byte DIMMs when they become available. |
| Flash Memory: | 1M byte of Intel 28F008 Flash memory standard. Built-in Vpp voltage generator. Provision to fit 2M byte 29F016 chip. |
| Printer port: | Centronics compatible (PRN). Bidirectional. EPP and ECP compatible. |
| Serial interface: | RS-232 (COM1 and COM2). RS-485 half-duplex option for COM2. |
| Keyboard port: | IBM AT compatible. |
| Mouse port: | PS/2 compatible. |
| Speaker port: | IBM AT compatible. |
| Reset circuit: | Power supply monitor, PC/104 bus reset, watchdog timer and external reset switch capability. |
| Bus interface: | PC/104 V2.3 16-bit |
| Interrupts: | Standard PC and PC/AT interrupts are available on the PC/104 bus, (IRQ 9 [IRQ2], IRQ3 to IRQ7, IRQ10, IRQll, IRQ14, IRQ15 and /IOCHCK). |
| DMA: | Standard PC and PC/AT DMA request and acknowledge pairs available on PC/104 bus. DREQ0 - 3, /DACK0 - 3 and DREQ5 - 7, /DACK5 -7. Multiple bus masters (using the /MASTER signal) are not supported. |
| Connectors: | Standard PC/104 8-bit and 16-bit stack-through connectors. A single 50-way I/O connector. A 4 way right angle Molex power connector. Non-stack-through connectors optionally available. |
| Dimensions: | PCB - 3.550 inches x 3.775 inches, (91.7 mm x 95.8 mm Approx.). Overall dimensions including connectors, 3.9 inches x 4 inches, (99mm x 101.6mm Approx.). Maximum height on the component side of the PCB is 11.5mm. |
| Weight: | 95g Approx. |
| Temperature: | 0 - 60º C operating. |
| Humidity: | 10% - 90% non-condensing. |
| Power Supplies: | +5V at 640mA - TC586 (TI80486DX2 @ 66MHz, 16M byte DRAM). See Table 1 for power consumption of other configurations. |

# APPENDIX B: TC586 SET-UP PROCEDURE.

The component placement diagram in Appendix C may be of help in locating components referred to in this appendix.

## B.1 DRAM CONFIGURATION

The standard TC586 product is delivered with no DRAM DIMM modules fitted as standard. Users may buy DIMM modules from DSP Design or fit their own (see section 2.3 for notes on DRAM speed).

DRAM should be 70ns or faster, and must be designed for 5V operation, not 3.3V. Table B1 lists suitable devices

Install your DRAM DIMM module in the TC586 DRAM socket, observing its polarity, and observing proper anti-static precautions. The DIMM socket has a lug which engages with a cutout on the module, which prevents incorrect installation.

| DRAM Size | Part No | Suitable Part No. |
|---|---|---|
| 4M Bytes | DD4 | Toshibai THL321050ATG-7 (-6) |
| 8M Bytes | DD8 | Toshibai THL322050ATG-7 (-6) |
| 16M Bytes | DD16 | Toshibai THL324050ABG-7 (-6) |
| 32M Bytes | DD32 | Dynamem MX0833D52UEG-60 |

Table B1 - DRAM Module Part Numbers

## B.2 INSTALLING THE PROCESSOR

Install the processor into its 169 pin PGA socket, observing its polarity and anti-static handling precautions. The processor needs to be installed so that the bevelled corner of the processor aligns with the bevelled silk-screen marking on the PCB. The standard configuration of the TC586 is for 3.45V processors. If your processor does not operate at 3.45V then some or all of solder links LK1, LK3 and LK6 may need to be changed. See section B.3 for details of these solder links. In addition, solder links LK4, LK5, LK7 and LK8 may need to be adjusted depending on processor type. Table B.2 lists suitable signals for some processors.

Users should make their own decision concerning cooling of the processor. The processors will dissipate between 1.5W and 5W, depending on processor type, operating voltage and speed (see Table 1 for overall power consumption - all except about l80mA of the supply current goes to the processor), and may get quite hot. Most chip manufacturers recommend a heatsink and/or a fan to keep the temperature of the processor down. The cooler the chip the better will be its reliability. A fan or fan and heatsink combination can be fitted to the processor, or a fan could be provided in the enclosure along with the PC/104 boards, or the enclosure could be designed so that part of the enclosure acted as the heat sink.

DSP Design can provide a heatsink and a heatsink/fan combination. See Appendix D for ordering information.

| Processor | Voltage | Link Settings | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | LK1 | LK3 | LK4 | LK5 | LK6 | LK7 | LK8 |
| I486DX-33 | 5V | Fit | 1-2, 5-6 | N/C | 1-2 | X | 2-3 | 1-2-3 |
| I486DX2-66 | | | | | | | | |
| TI486DX2-66 | 3.45V | N/C | 2-3, 4-5 | | | Fit | | 1-3 |
| TI486DX2-80 | | | | | 2-3 | | 1-2 | |
| TI486DX4-100 | | | | | 1-2 | | 2-3 | |
| ST486DX2-66 | 5V | Fit | 1-2, 5-6 | | | X | | |
| ST486DX2-80 | | | | | 2-3 | | 1-2 | |
| ST486DX4-100 | 3.45V | N/C | 2-3, 4-5 | | 1-2 | Fit | 2-3 | 1-2-3 |
| ST5x86-100 | | | | | | | | |
| AM486DX4-100 | 3.3V | | | | | N/C | | |
| AM486DX4-120 | | | | | 2-3 | | 1-2 | |
| AM5x86-133 | 3.45V | | | Fit | 1-2 | Fit | 2-3 | |

Table B2: Link settings for some processors (Rev C Boards only)
(N/C = no connection, X = don't care)

### B.3 SOLDER LINK AREAS

A number of functions can be configured with solder links on the TC586 board. The board layout is so dense we have implemented these configuration options with solder links which take less space than jumpers as well as being more reliable.

Care must be taken when changing these link areas so that no accidental shorts are produced or created. Default settings are noted below.

Note that there are some differences (at LK3 and LK8) between REV B and REV C versions of the TC586. These are noted below. REV B boards can be identified by the text “176001.B00” on the PCB copper, underneath the DIMM memory module. REV C boards have “176001.C00” in this position.

#### LK1 PROCESSOR VOLTAGE SELECTION

This link needs to be set to provide the processor with the correct supply voltage.

| | |
|---|---|
| For 5V processors: | Install link. |
| For 3.3V processors: | Do not install link. (Default setting) |
| For 3.45V processors: | Do not install link. (Default setting) |

#### LK2 COM2 RS-232/RS-485 SELECTION

This link is used to select whether COM2 is RS-232 or RS-485.

| | |
|---|---|
| RS-232: | Link 1-2 (Default setting) |
| RS-485 | Link 2-3 |

### LK3 PROCESSOR VOLTAGE SELECTION

This link needs to be set to provide the processor with the correct supply voltage.

On REV B boards:

| | |
|---|---|
| For 5V processors: | Link 1-2, and remove IC10 (LTC1430) |
| For 3.3V processors: | Link 2-3 (Default setting) |
| For 3.45V processors: | Link 2-3 (Default setting) |

On REV C boards:

| | |
|---|---|
| For 5V processors: | Link 1-2 and 5-6 |
| For 3.3V processors: | Link 2-3 and 4-5 (Default setting) |
| For 3.45V processors: | Link 2-3 and 4-5 (Default setting) |

### LK4 PROCESSOR CLOCK MULTIPLIER

Most processors have an internal clock multiplier, which multiplies the local bus clock frequency internally, typically by a factor of 2, 2.5 or 3. This link is connected the CLKMUL pin (pin R17) on these processors, and connects the pin to GND (logic 0) when the link is made.

This link needs to be set to match the processor used. Table B.1 gives suitable settings for some processors.

### LK5 LOCAL BUS FREQUENCY

LK5 and LK7 are used together to set the frequency of the local bus clock, accordingly to the table below:

| Frequency | LK5 | LK7 |
|---|---|---|
| 16MHz | 1 - 2 | 1 - 2 |
| 25MHz | 2 - 3 | 2 - 3 |
| 33MHz | 1 - 2 | 2 - 3 |
| 40MHz | 2 - 3 | 1 - 2 |

Table B3: Local Bus Frequency Settings (default setting shown shaded)

### LK6 PROCESSOR VOLTAGE SELECTION

This link needs to be set to provide the processor with the correct supply voltage.

| | |
|---|---|
| For 5V processors: | Position is don’t care. |
| For 3.3V processors: | Do not link |
| For 3.45V processors: | Install link. (Default setting) |

### LK7 LOCAL BUS FREQUENCY

See LK5 above.

### LK8 RESET SOURCE

This link needs to be set to match the processor used. Table B.2 gives suitable settings for some processors on the REV C PCB.

On the REV B board this should be set for 1 - 2, but note that Texas Instruments and 5V SGS Thompson processors cannot be used on the REV B board.

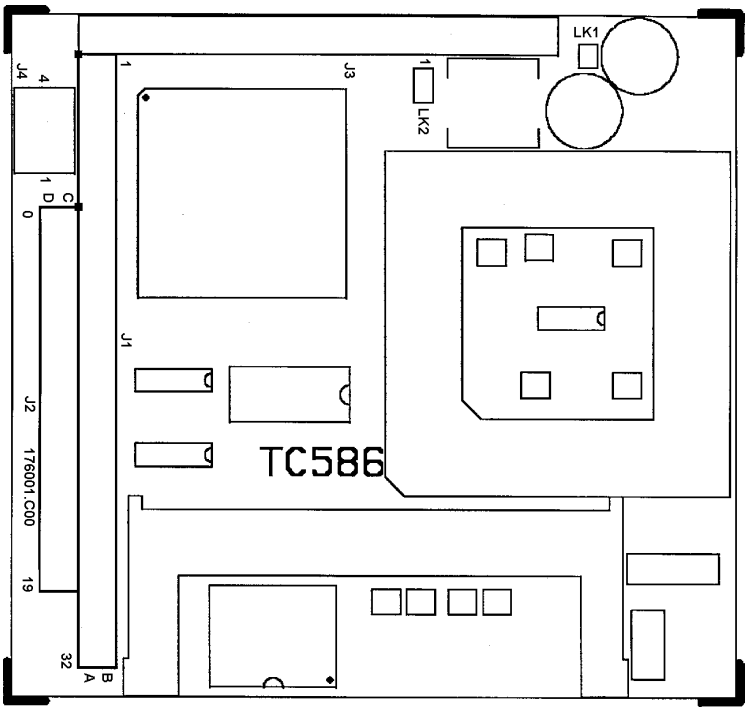
### LK9 REMOTE BOOTSTRAP

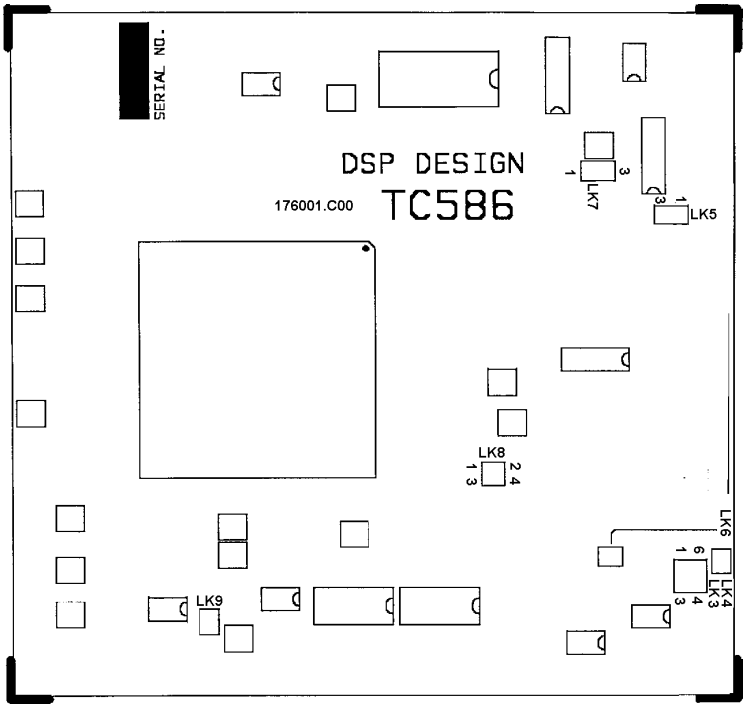
This link needs to be set according to the location of the BIOS. It is normally only used in the manufacturing process.

| | |
|---|---|
| BIOS is in the Flash memory: | Install link. (Default setting) |
| BIOS is in off-board EPROM: | Do not install link. |

## APPENDIX C: COMPONENT PLACEMENT DIAGRAMS

The two component placement diagrams which follow (one for each side of the TC586) may be of help in locating the components referred to in Appendix B.



## APPENDIX D: OPTIONS AND ORDERING INFORMATION

This Appendix lists some of the range of PC/104 products available from DSP Design, and in particular the products related to the TC586. Note that as new products are being released all the time this list may not be complete. Contact your supplier for a full price list.

The standard TC586 is fitted with no processor or DRAM. Options which can be added to the base unit are detailed below.

PROCESSOR BOARD

| | |
|---|---|
| TC586 | Standard TC586 processor board, without processor or memory. |

DRAM

| | |
|---|---|
| DD4 | 4M byte DIMM DRAM module |
| DD8 | 8M byte DIMM DRAM module |
| DD16 | 16M byte DIMM DRAM module |
| DD32 | 32M byte DIMM DRAM module |

PROCESSORS

| | |
|---|---|
| TI486DX2-66 | 486DX2-66 - local bus clock 33MHz, internally 66MHz (3.45v) |
| TI486DX2-80 | 486DX2-66 - local bus clock 40MHz, internally 80MHz (3.45v) |
| TI486DX4-100 | 486DX4-100 - local bus clock 33M Hz, internally 100M Hz (3.45v) |
| AMD486DX5-133 | 5x86-133 - local bus clock 33MHz, internally 133MHz (3.45V) |

ACCESSORIES

The following part numbers should be used to order various accessories:

| | |
|---|---|
| TCPAK586 | Starter pack including TC586, TCDEV, TC586-UTILS, TRM-TC586 and TCPSU. Processor chip and DRAM are ordered separately |
| TC586-UTILS | Utilities disk for TC586 |
| TRM-TC586 | Technical reference manual |
| TCDEV | PC/104 Development Platform |
| TCPSU | Power supply unit for the TCDEV |
| TCDOS | Microsoft MS-DOS Operating System |
| TCWIN | Windows operating system |
| TC586HS | Heatsink and thermally conductive double-sided adhesive tape, to attach to a processor. |
| TC586FAN | Heatsink and thermally conductive double-sided adhesive tape, to attach to a processor. |
| TCSPACER | PC/104 spacer kit - four 0.6 inch spacers plus nuts and washers. |
| COMMDOS-DRV | DOS Serial Communications Driver Software |
| TCDISK-810 | 2½" IDE drive for the TCDEV |
| IDE-3020 | Cable to convert 2½ inch IDE connector to 3½ inch IDE connector and vice-versa |

### PC/104 MODULES

The following list describes a selection of the PC/104 bus cards that are available from DSP Design. Contact your supplier for the latest list.

### I/O MODULES

| | |
|---|---|
| TSYST | System I/O board, comprising serial ports, parallel port, floppy & hard disk drive controller. Can be used to provide floppy and IDE disk drives for the TC586. |
| TV750 | Super VGA interface board. Supports simultaneous CRT and flat panel displays. |
| TCMCIA-2 | Two slot PCMCIA interface card. |
| TP024 | Opto-isolated I/O board. Twelve inputs and twelve outputs |
| TP406 | Parallel I/O and timer board. Forty lines of parallel I/O |
| TENET | Ethernet interface card |
| TS400 | Four serial interfaces on one card |
| TAD12 | 12-bit Analogue to Digital converter card |

FLASH DISKS

Tiny Flash Disks are PC/104 modules which can be added to the TC586 to provide Flash File System memory in excess of that provided by the on-board Flash chip.

| | |
|---|---|
| TFD-01 | 1M byte PC/104 flash disk module (small format) |
| TFD-02 | 2M byte PC/104 flash disk module (small format) |
| TFD-04 | 4M byte PC/104 flash disk module (small format) |
| TCFL01M | 1M byte PC/104 flash disk module |
| TCFL02M | 2M byte PC/104 flash disk module |
| TCFL04M | 4M byte PC/104 flash disk module |
| TCFL08M | 8M byte PC/104 flash disk module |
| TCFL16M | 16M byte PC/104 flash disk module |
| TCFL32M | 32M byte PC/104 flash disk module |

# APPENDIX E: CONNECTOR PIN ASSIGNMENTS

## E.1 TC586 PERIPHERAL CONNECTORS

The peripheral devices are connected to the TC586 through a 50 way IDC connector, called J3. The 50 pins on the connector are brought to the outside world through a 50 way 0.1 inch IDC right angled connector. Note that pins 1 and 2 differ between REV B and REV C versions of the TC586. REV B boards can be identified by the text “176001.B00” on the PCB copper, underneath the DIMM memory module. REV C boards have “176001-C00” in this position. These pins (pins 1 and 2) are the only pins on the J3 connector which differ from the TC386 and TC486 boards. Users who are updating from TC386 or TC486 boards should note this.

Table E1 lists the J3 signal name and also the peripheral to which the signal belongs and the pin number of that peripheral’s connector. The standard connectors used in PC’s for each of the peripherals are:

| | |
|---|---|
| Centronics Printer: | 25 way female D-type |
| Keyboard: | 5 way female circular DIN |
| Mouse: | 6 pin mini DIN (PS/2 style) |
| Serial COM1: | 9 way male D-type |
| Serial COM2: | 9 way male D-type |
| Loudspeaker: | N/A |
| Battery: | N/A |
| Reset Switch: | N/A |

Pin 1 of the J3 connector can be identified by looking at the J3 silk-screen box which surrounds the J3 connector on the TC586. A “ 1 “ is located close to the pin 1 end of J3 and a “49” is placed close to the pin 50 end. All odd numbered pins are in one row and all even numbered pins are in the other row.

| Pin | Peripheral | Signal | J3 | J3 | Signal | Peripheral | Pin |
|---|---|---|---|---|---|---|---|
| | | IRRX | 1 | 2 | IRTX | | |
| 5 | Mouse | MCLOCK | 3 | 4 | MDATA | Mouse | 1 |
| 13 | Centronics | SLCT | 5 | 6 | PE | Centronics | 12 |
| 11 | | BUSY | 7 | 8 | /ACK | | 10 |
| 9 | | PD7 | 9 | 10 | PD6 | | 8 |
| 7 | | PD5 | 11 | 12 | PD4 | | 6 |
| * | | GND | 13 | 14 | PD3 | | 5 |
| 17 | | /SLCTIN | 15 | 16 | PD2 | | 4 |
| 16 | | /INIT | 17 | 18 | PD1 | | 3 |
| 15 | | /ERROR | 19 | 20 | PD0 | | 2 |
| 14 | | /AUTOFD | 21 | 22 | /STROBE | | 1 |
| | Reset | GND | 23 | 24 | /RESET | Reset | |
| | Speaker | VCC | 25 | 26 | SPKR | Speaker | |
| | Battery | GND | 27 | 28 | BATT | Battery | |
| 5 | Keyboard | VCC | 29 | 30 | KBDATA | Keyboard | 2 |
| 4 | | GND | 31 | 32 | KBCLK | | 1 |
| 5 | Com2 | GND | 33 | 34 | RI1 | Com2 | 9 |
| 4 | | DTR1 | 35 | 36 | CTS1 | | 8 |
| 3 | | TXD1 | 37 | 38 | RTS1 | | 7 |
| 2 | | RXD1 | 39 | 40 | DSR1 | | 6 |
| 1 | | DCD1 | 41 | 42 | GND | Com1 | 5 |
| 9 | Com1 | RI0 | 43 | 44 | DTR0 | | 4 |
| 8 | | CTS0 | 45 | 46 | TXD0 | | 3 |
| 7 | | RTS0 | 47 | 48 | RXD0 | | 2 |
| 6 | | DSR0 | 49 | 50 | DCD0 | | 1 |

Table E3 - J3 I/O Connector Pin assignments

* J3 pin 13 connects to Centronics Port pins 18 to 25 inclusive.
Pins 37 and 38 carry RS-485 inverting and non-inverting data, respectively,
when Com2 operates as an RS-485 port.

### E.2 J4 POWER CONNECTOR

The J4 connector is used to provide an alternate power inlet to the TC586 for stand alone operation. The J4 connector uses industry standard parts and a number of manufacturers are able to provide suitable mating connectors.

The J4 connector used on the TC586 is a Molex mini KK, 2.5mm pitch, 5046 series right angled header with friction lock. A suitable mating half would be the MOLEX mini KK 2.5mm pitch 5051 series crimp polarizing housing. Crimp pins are required for this housing connector and these are also available from Molex. At the time of writing Farnell Electronic Services supply these Molex parts as standard with the stock numbers 011-007D for the polarized housing connector and 011-122R for the crimp pins.

| J4 Pin | Signal |
|---|---|
| 1 | GND |
| 2 | |
| 3 | Vcc |
| 4 | |

Table E2: J4 Power Connector Pin Assignments

Pin 1 of the J4 connector can be identified by looking at the silk-screen ident on the TC586 PCB. Pin 1 has a ’1’ to the right hand side of the connector.

## E.3 BUS CONNECTORS

The PC/104 bus connector pin assignments conform to the PC/104 bus specification V2.3. The pin assignment is shown below.

| Pin | J1 | |
|---|---|---|
| | Row A | Row B |
| 1 | /IOCHCHK | 0V |
| 2 | SD7 | RESETDRV |
| 3 | SD6 | +5V |
| 4 | SD5 | IRQ9 |
| 5 | SD4 | -5V * |
| 6 | SD3 | DRQ2 |
| 7 | SD2 | -12V * |
| 8 | SD1 | /ENDXFR |
| 9 | SD0 | +12V * |
| 10 | IOCHRDY | (KEY) |
| 11 | AEN | /SMEMW |
| 12 | SA19 | /SMEMR |
| 13 | SA18 | /IOW |
| 14 | SA17 | /IOR |
| 15 | SA16 | /DACK3 |
| 16 | SA15 | /DRQ3 |
| 17 | SA14 | /DACK1 |
| 18 | SA13 | DRQ1 |
| 19 | SA12 | /REFRESH |
| 20 | SA11 | SYSCLK |
| 21 | SA10 | IRQ7 |
| 22 | SA9 | IRQ6 |
| 23 | SA8 | IRQ5 |
| 24 | SA7 | IRQ4 |
| 25 | SA6 | IRQ3 |
| 26 | SA5 | /DACK2 |
| 27 | SA4 | TC |
| 29 | SA3 | BALE |
| 29 | SA2 | +5V |
| 30 | SA1 | OSC |
| 31 | SA0 | 0V |
| 32 | 0V | OV |

| Pin | J2 | |
|---|---|---|
| | Row C | Row B |
| 0 | 0V | 0V |
| 1 | /SBHE | /MEMCS16 |
| 2 | LA23 | /IOCS16 |
| 3 | LA22 | IRQ10 |
| 4 | LA21 | IRQ11 |
| 5 | LA20 | IRQ12 |
| 6 | LA19 | IRQ15 |
| 7 | LA18 | IRQ14 |
| 8 | LA17 | /DACK0 |
| 9 | /MEMR | DREQ0 |
| 10 | /MEMW | /DACK5 |
| 11 | SD8 | DRQ5 |
| 12 | SD9 | /DACK6 |
| 13 | SD10 | DRQ6 |
| 14 | SD11 | /DACK7 |
| 15 | SD12 | DRQ7 |
| 16 | SD13 | +5V |
| 17 | SD14 | /MASTER* |
| 18 | SD15 | 0V |
| 19 | (KEY) | 0V |

Table E3: J1/P1 and J2/P2 Bus Connector Pin Assignments

Pins 1 and 32 of J1 connector is marked on the PCB silk-screen with a ‘l” and “32” respectively, and rows A and B are also marked. (Note - due to a PCB design error the text on the silk screen of some TC586 boards shows J1 as having rows A and C (which is incorrect), rather than rows A and B (which is correct). Pins 0 and 19 of J2 connector are marked on the PCB silk-screen with a “0” and “19” respectively, and rows C and D are also marked.

# APPENDIX F: DIFFERENCES BETWEEN TC586 AND TX486

## F.1 SUMMARY OF DIFFERENCES

All features not mentioned in the Appendix remain unchanged between the TX486 and TC586. The TX486 differs from the TC586 in the following ways:

- **Processor is changed from a PGA package to a PQFP package. The processor is thus fitted at build time, rather than by the customer.**
- **Flash memory options have been extended. As well as the options for a single 1 M byte or 2M byte flash chip, a second 1 M byte or 2M byte Flash chip can now be fitted. A 128k or 256k byte chip can also be fitted as an alternative.**
- **IDE and floppy disk interfaces have been added to the TX486. The IDE drives connect through a 2mm 44-pin connector. The floppy drive connects through a 26way flat flexible cable.**
- **A linear voltage regulator can optionally replace the switch mode power supply.**
- **A two-pin connector has been provided for an optional fan.**
- **Improved noise performance on the /RESET input.**
- **The A19 mask mechanism has been changed to improve operation.**
- **Some bits in the Utility Register have been redefined to accommodate the extra 2M bytes of Flash memory.**

## F.2 PROCESSOR

The most significant change from the TC586 is to replace the processor in a PGA package with a processor in a Plastic Quad Flat Pack (PQFP) package. This is the method by which board space has been freed to add the IDE interface.

The PQFP package is available from Intel and AMD. DSP Design fit a 100MHz AMD 486DX4-100 as standard. Also available are a 66MHz 486DX2 (clock-doubled) and a 133MHz 486DX5 (clock-quadrupled) parts. All operate at 3.3V.

The processor is fitted on the rear of the board. A connector has been added close to the processor which could be used to power a fan.

## F.3 FLASH MEMORY

The TX486 has the ability of being populated with a number of different Flash memory chips. The memory fitted can be chosen to optimise the cost of the board.

The board can accept any of the following:

- A 128k byte flash chip (28F010). This would be suitable for systems which boot from hard disk, and which do not require ROM disk or a Flash File System.
- A 256k byte flash chip (28F020).
- One or two 1M byte flash chips (28F008). This is suitable for ROM disks or Flash File Systems.

- One or two 2Mbyte flash chips(29F016).This is suitable for larger ROMdisks to a maximum capacity of 4M bytes.

The standard configuration is for a single 29F016 to be fitted, providing 2M bytes of flash memory.

### F.4 IDE INTERFACE

An IDE disk interface is provided on the TX486. This performs in a similar way to the TC586 with a TSYST or alternative IDE interface; ie, two drives are supported, which can be either hard disk drives or CD-ROMS; and capacities in excess of 520M bytes are supported (MS-DOS places a 2G byte limit).

A 44-way connector on 2mm pitch is provided. This is a straight surface mount connector, located on the edge of the board opposite the 50-way I/O connector.

### F.5 FLOPPY DISK INTERFACE

A floppy disk interface has been added to the TX486. The 87306 Super I/O chip includes the floppy disk interface circuitry, and a floppy disk can now be connected to it through a 26-way connector flat flexible cable. This cable type is used on some low profile 3.5" floppy disk drives. The drives and the cables are available from your supplier.

### F.6 MECHANICAL INTERFACE

The positions of the existing connectors and mounting holes are the same as the TC586. The pin assignments of the common connectors are the same.

There are three new connectors on the TX486. All are contained within the border of the PCB. The IDE interface is implemented with a 44-way 2mm pitch straight connector on the edge opposite the current 50-way I/O connector. A floppy disk interface is implemented with a 26-way flat flexible cable, which is located on the edge of the PCB opposite the PC/104 connectors. A fan could be powered from a two-pin friction-lock connector, on the same edge as the floppy connector.

The DIMM memory module has moved further onto the board, to make space for the IDE connector. The processor has moved to the rear of the PCB.

Solder links on both boards have the same functions and names, although some links which are not required on the TX486 have been omitted. Connectors which are present on both boards have the same names, positions and pin assignments. Other components are re-numbered.

### F.7 POWER CONSUMPTION

The power supply requirements of the TC586 and TX486 are almost identical, for a given processor and clock speed. (The power consumption varies depending on processor type and clock frequencies). Power consumption figures are given in Table 1.

> Note that the Table I figures were made with a 4M byte DIMM module fitted, and power consumption may be higher when other amounts of DRAM is fitted.

Heatsinks are available for the PQFP package, and alternative cooling fins are also available.

### F.8 LINEAR VOLTAGE REGULATOR

The switch mode power supply circuitry on the TC586 and TX486 boards contributes not insignificantly to the cost of the boards, although the overall power consumption is reduced as a consequence.
Provision has been made on the TX486 for an alternative linear voltage regulator, which could be fitted when cost savings are required and where the extra power consumption is not an issue. The voltage regulator will require an external heatsink. It is positioned on the edge of the PCB, which may allow the case to be used as a heatsink in som6 systems. The use of the linear voltage regulator is subject to a minimum order quantity.

### F.9 A19 MASK MECHANISM

As reported in section 2.5 of the TC586 Technical Reference Manual, the 64k bytes of the PC/104 bus memory address space at E0000h cannot currently be used on the TC586, unless BIOS code (not currently implemented) manipulates the /A19LOW bit in the Utility Register. This is due to a conflict between PC/104 memory at E0000h and the on-board flash memory, which temporarily occupies E0000h following reset.

The way the PC/104 A19 bit is manipulated has been changed on the TX486, so that the PC/104 bus memory space at E0000h can be used with the TX486.

No changes to software are required.

### F.10 IMPROVED NOISE PERFORMANCE ON /RESET PIN

The noise immunity on the /RESET pin (on the J3 I/O connector) has been improved on the TX486, by fitting a gate with hysteresis on this line.

### F.11 FAN CONNECTOR

A two-pin friction-lock connector has been added on the TX486. It carries +5V and GND power connections, and could be used to power a fan if required.

### F.12 DIFFERENCES IN UTILITY REGISTER PIN ASSIGNMENTS

The addition of an extra 2M bytes of Flash memory on the TX486 requires an additional address bit to address the Flash memory. This bit is provided by the Utility Register, described in section 3.11 of this manual. Thus the function of some bits in the Utility Register differs between the two boards, and software must be adjusted as well, if the extra 2M bytes of Flash memory are required.

Bits which are changed are given in Table Fl.

| Bit | Port | TC586 Function | TX486 Function |
|---|---|---|---|
| 3 | ECh | /A19LOW | Version ID - connect to Bit 3 Port EDh |
| 3 | EDh | BA17 | BA17 and Version ID - connects to Bit 3 Port ECh |
| 7 | EDh | /SLOWCLK | BA21 |

Table F1: Changes to Utility Register Bits

Note that /AI9LOW and /SLOWCLK were not used on the TC586, so changing their function on the TX486 will not remove any existing TC586 functionality. Furthermore, the new functions of the bits will not affect the functioning of existing TC586 software, since existing TC586 software leaves the /AI9LOW and /SLOWCLK bits as logic 1 (the state following reset), which is satisfactory for operation on the TX486.

The TC586 /SLOWCLK bit becomes the TX486 BA21 - the extra address bit required if the second 2M byte Flash chip is fitted. This bit is left high on boards with only one Flash chip, and while accessing the first Flash chip on boards with two Flash chips. It is only taken low to access the second Flash chip on boards which have two fitted. It must not be taken low on TC586 boards.

While TC586 software will operate on the TX486 board, it will be necessary to know which version board is in use prior to taking the BA21 bit low. This is done by linking the TC586 /A19LOW bit to the BA17 bit. The /A19LOW bit is not required on the TX486 for masking the A19 bit (its intended use on the TC586). Thus it can be redeployed on the TX486 as a version identification bit.

To identify the TX486, software can toggle the BAI7 bit, and see whether Bit 3 of Port ECh changes in response. If the bit does change then the TX486 is identified, and software can thus use Bit 7 Port EDh as BA21. If it does not change then a TC586 is present and Bit 7 of Port EDh has a /SLOWCLK function.

In summary, TC586 Flash programming software should continue to work on the TX486 in all cases except where access to the second Flash chip is required. Furthermore, it is possible to write new versions of Flash programming software that can determine whether it is running on the TX486 or on a TC586, and thus access the second Flash chip if appropriate. This is what we have done with the Flash programming programs and the Flash File System, which operate on both the TX486 and the TC586.

It will be possible to connect other BA bits to Bit 3 Port ECh on possible future versions of the board, thus identifying the future versions as well.

Software which was written for the TC586, which accesses the Flash memory will have to change if the second 2M byte Flash chip is installed, as described in section 4.5. If the second 2M byte Flash chip is not installed then old TC586 software should run without change.

### F.13 BIOS

The TX486 BIOS differs slightly from the TC586, in order to enable access to the IDE and/or floppy disk controllers.

# APPENDIX G: POWER SAVING OPTIONS

Sometimes significant power savings can be realised by reducing the processor system speed or by causing the processor to enter a power down state when idle. Two features exist with the TC586 and AMD processor combination that allow us to investigate these possibilities.

## G.1 AMD PROCESSOR - AUTO HALT POWER DOWN STATE

The AMD processor includes an *Auto Power Down State* feature. This allows us to explore the power saving capabilities of the AMD CPU.

An 80x86 HLT (halt) instruction causes the AMD CPU to enter an *Auto Power Down* State. The CPU issues a normal halt bus cycle and only transitions to the normal state when INTR, NMI, /SMI, RESET or SRESET occurs.

While the processor is held in a halted state power consumption is significantly reduced (See table 1 below). Note that in a DOS environment the system timer tick will generate an interrupt every 18.2Hz. This interrupt will reset the halt power down state returning the CPU to normal operation. For the purposes of this test the processor will be forced to execute HLT instructions in a continuous loop.

Tests were performed with the TC586 configured as follows: TC586, 4M bytes DRAM and an AMD486DX5-133 processor.

The results of the test are given in Table Fl.

| Mode of operation | Current Drawn mA |
|---|---|
| Normal | 1030 |
| Auto Halt Power Down | 158 |
| Power.exe running | 168 |

Table G1: Power Saving Modes

## G.2 MSDOS - POWER.EXE UTILITY

Later revisions of MS-DOS provide a power saving utility designed primarily for laptop computers to help reduce power consumption and conserve battery power. POWER.EXE is installed as an MS-DOS device driver and once loaded remains memory resident. It works by checking for application or hardware activity. If there is no activity the power saving code is triggered and processor power consumption falls.

The MS-DOS POWER.EXE utility is simple and easy to implement and is recommended for most power saving requirements.

The various advanced parameters of the POWER.EXE utility have virtually no effect on power consumption with the TC586 because the TC586 BIOS does not implement Advanced Power Management (APM) features.

To install the POWER.EXE utility onto your TC586 system edit your MS-DOS CONFIG.SYS file and add the following line (assumes that POWER.EXE is in a directory called C:\DOS):

```
DEVICE=C:\DOS\POWER.EXE
```

You will be required to re-boot the TC586 system for the new settings to take effect.

### G.3 HALTING OTHER PROCESSORS

The following table contains power consumption figurers for a variety of 3.3V and 3.45V processors. For the purposes of this test the processor was forced to execute HLT (halt), instructions in a continuous loop.

| Processor | Voltage | Normal Current | Halt Current |
|---|---|---|---|
| AMD486DX5-133 | 3.45 | 1030 | 158 |
| AMD486DX4-120 | 3.3 | 1130 | 162 |
| ST5x86-100 | 3.45 | 990 | 650 |
| ST486DX4-100 | | 794 | 518 |
| TI486DX4-100 | | 730 | 466 |
| TI486DX2-66 | | 539 | 355 |

### G.4 SYSTEM WAIT TIMER

Small power savings can be made by using a feature exclusive to the FTD4591 system controller chip. The FTD4591 includes a programmable wait timer that allows transparent hardware control of the system speed. By using this feature we can measure power consumption with varying system speed settings.

The wait timer is controlled by bits 3-6 of the miscellaneous register (Read/Write I/O 0FC2Fh). When the wait timer is enabled (bit 3=1), the processor is allowed to run for 1µS, then the CPU generates a hold request. The CPU is kept in the hold condition for a programmable period between 1µS and 16µS, then control is returned back to the CPU for 1µS. The cycle repeats itself until the wait timer is disabled (bit 3=0). Bits 4-6 of the miscellaneous register are used to program the hold period from between 1µS and 16µS. All other Bits in this register should remain unchanged.

By effectively reducing the CPU speed, power consumption is slightly reduced (figures for three settings are shown below).

| Mode of operation | Current Drawn mA |
|---|---|
| Normal | 1030 |
| System Wait Timer - 1uS | 998 |
| System Wait Timer - 4uS | 952 |
| System Wait Timer - 16uS | 914 |

Table G2: System Wait Timer Power Savings

### G-5 SUMMARY

The Auto Halt Power Down State feature of AMD Processors can help significantly in reducing Power consumption. However since the Processor cannot execute instructions while halted the method of returning to normal operation must come from either an interrupt (INTR, NMI or /SMI) or a system reset.

Alternatively the MSDOS POWER.EXE utility can be used to automatically reduce power consumption when the application or hardware is idle, returning to normal operation automatically. The POWER-EXE utility makes use of the halt features mentioned in this document.

The System Wait Timer allows a small reduction in power consumption while maintaining normal program execution. Normal that is, except for a significant drop in system speed and therefore overall system performance.

The MS-DOS POWER.EXE utility is recommended in most cases as this is an established piece of software supported by Microsoft and requires no customer application code modifications for implementation.

## APPENDIX H: FAULT REPORTING

DSP Design makes every effort to ship products and documentation which are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a “Product Fault Report" form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form to your supplier.

Prior to returning a faulty product, please check the following:

1 The board has been correctly configured for the intended application (see earlier appendix for board installation details).

2. The power supplies are providing correct voltage levels.

3. Cabling to the board is sound and connected correctly.

4. Other cards in the system are known to be correctly configured and functioning.

5. **PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

*Your help with this will enable us* to *sort out your problem more quickly. Thank you.*

## PRODUCT FAULT REPORT

CUSTOMER INFORMATION
COMPANY NAME:
INDIVIDUAL CONTACT:
PHONE NO:

PRODUCT INFORMATION
PRODUCT/DOCUMENT:
SERIAL NO:
DATE OF RETURN:

---

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

---

IN WHAT CONFIGURATION IS THE BOARD USUALLY USED? (WHAT OTHER BOARDS, WHAT SOFTWARE ETC)?

---

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT:

REPAIRED BY:

CHARGES TO BE INVOICED: E

DATE OF RETURN:

RETURNED BY: